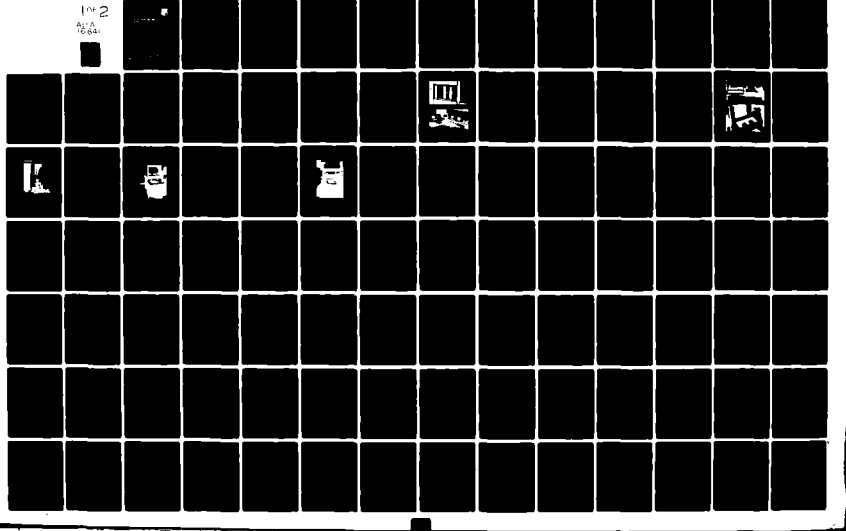
AD-A116 841 TRW DEFENSE AND SPACE SYSTEMS GROUP MCLEAN VA F/G 15/7
TACTICAL OPERATIONS ANALYSIS SUPPORT FACILITY,(U)
MAY 82 M P MURPHEY, D E YUCHNOVICZ, R W STARR F30602-78-C-0196
UNCLASSIFIED RADC-TR-82-15 NL



(12)

RADC-TR-82-15
Interim Report
May 1982

TACTICAL OPERATIONS ANALYSIS SUPPORT FACILITY

TRW Defense and Space Systems Group

Michael P. Murphey
Daviel E. Yuchnovicz
and Roger W. Starr

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-82-15 has been reviewed and is approved for publication.

APPROVED: Dennis R. Nawoj

DENNIS R. NAWOJ
Project Engineer

APPROVED: John N. Entzminger Jr.

JOHN N. ENTZMINGER, JR.
Technical Director
Intelligence and Reconnaissance Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (IRDE) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document requires that it be returned.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-82-15	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) TACTICAL OPERATIONS ANALYSIS SUPPORT FACILITY		5. TYPE OF REPORT & PERIOD COVERED Interim Report 1 Jul 80 - 30 Jun 81
		6. PERFORMING ORG. REPORT NUMBER N/A
7. AUTHOR(s) Michael P. Murphey Daviel E. Yuchnovicz Roger W. Starr		8. CONTRACT OR GRANT NUMBER(s) F30602-78-C-0196
9. PERFORMING ORGANIZATION NAME AND ADDRESS TRW Defense and Space Systems Group 7600 Colshire Drive McLean VA 22102		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 63789F 23150221
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (IRDE) Griffiss AFB NY 13441		12. REPORT DATE May 1982
		13. NUMBER OF PAGES 100
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Same		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Dennis R. Nawoj (IRDE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Computer system hardware	Fiber optics technology
Computer system software	Winchester disk
Automated Data Processing Facility	Color graphics systems

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the current computer hardware and operating system software configuration of the Tactical Operations Analysis Support (TOAS) Facility at Langley AFB VA. The TOAS is the focal point for test and evaluation activities sponsored by RADC Project 2315, Automated Tactical Intelligence. Project 2315 is directed at developing new and improved automation techniques and procedures to enhance tactical operational intelligence support. The current report updates and expands last year's

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

interim technical report and provides Project 2315 contractors and other government users with the hardware and software technical specifications documentation. This documents reports on the Winchester Disk and fiber optics technologies implemented at the facility. These two technologies will have major impact on large scale data bases, tactical (mobile) systems, and security system implementation.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS AND TABLES

1. INTRODUCTION

The Tactical Operations Analysis Support (TOAS) Facility is an advanced development effort sponsored by the Rome Air Development Center (RADC) as part of Project 2315 - Automated Tactical Intelligence. The primary objective of the TOAS Facility effort is to provide a computer hardware and software environment to support the automation demonstrations and experiments of the other Project 2315 contractors and government agencies. The final goal of Project 2315 is to provide the design specifications for an automated Tactical Air Intelligence System (TAIS) to support tactical Air Force operations in the 1990 timeframe. This interim report documents the new TOAS Facility hardware and software tools and new technology implemented/suggested for the TOAS Facility.

1.1 TACTICAL OPERATIONS ANALYSIS SUPPORT (TOAS) FACILITY

A direct approach was used to implement the TOAS Facility requirement for automated R&D tools for developing, evaluating, and testing

- Software systems,
- Hardware Components, and
- Functional Procedures.

The Facility was located at Langley Air Force Base, Virginia, in order that the Air Force user could readily be a major participant in the R&D process. This close user-developer relationship provides better functional requirement definition and valuable user comment/guidance for on-going R&D efforts.

The current Facility configuration consists of two DEC PDP-11/70 computers, system peripherals, and graphics display devices (SU 1652, Imlac PDS-4, and CGC-7900 color). A Bunker Ramo multiplexer is also available. As new hardware and system software needs are evolved, the Facility computer environment will be changed to support the new

requirements. This document provides a technical description of the new computer resources and technology implemented at the Facility since publication of last years report. For completeness and continuity, the management Plan and brief descriptions of all other automated tools are also included.

1.2 TOAS FACILITY TECHNICAL REPORT

The purpose of this interim report is to update and expand the TOAS Baseline Interim Technical Report dated January 1981. Section 2 is a technical description TOAS hardware and software modules; more technical detail is provided on those equipments added since last year. This section provides a common baseline for personnel using the TOAS Facility. Section 3 is an updated TOAS Facility Management Plan. This Plan details the TOAS Facility operating procedures/practices and establishes Facility management responsibilities and system configuration guidelines. Section 4 is an overview of several technologies (Winchester, fiber optics, DBMS machines, and 32 bit mini/micro computers).

2. TOAS FACILITY SYSTEM ENVIRONMENT

This section provides the current TOAS Facility configuration and technical descriptions of the hardware and system software resources. This report details the equipment/technology added since publication of last years report. Project 2315 and other Air Force sponsored R&D projects use this facility to test and demonstrate software and hardware technologies to support the Tactical Intelligence arena. This section is provided as documentation of the hardware and software tools available at the Facility. If required, additional technical data is available from the on-site TRW representatives and the manufacturer's technical documentation available at the TOAS facility.

The TOAS Facility consists of dual PDP 11/70 computers, system support peripherals, and various user interface devices. The computers are currently operating in autonomous modes to support a dedicated system (System A) for specific functional demonstration/experimentation work and a software development timesharing system (System B). The overall Facility configuration is provided in Figure 2-1. Systems A and B are detailed in Figures 2-2 and 2-3 respectively. A Facility hardware list is in Table 2-1.

2.1 BASELINE HARDWARE DESCRIPTION

The major features of the computer hardware are documented in this section. Additional information is available from RADC-TR-81-99.

2.1.1 Central Processing Unit

The PDP-11/70 Central Processing Unit (CPU) is the KWB11-C 16 bit processor intended for high-speed, real time applications, and for large multi-user, multi-task, time sharing applications. Memory management allows 16, 18, and 22-bit addressing modes for operating systems and tasks requiring large amounts of addressable memory. Integral components of the CPU include: Cache Memory organization to provide a high-speed memory; FP11-C floating-point processor; and Memory Management for relocation and protection in multi-user, multi-task environments.

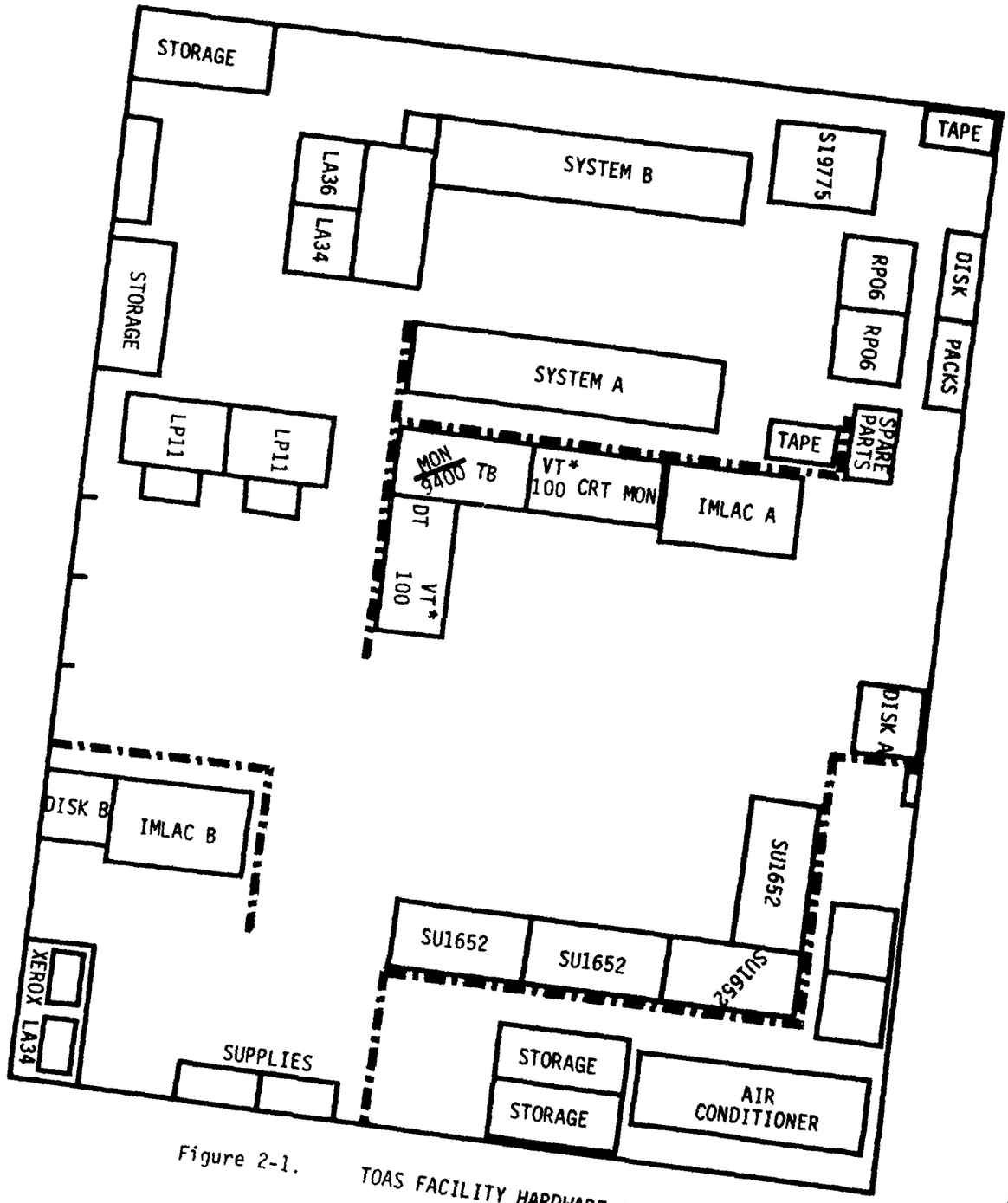
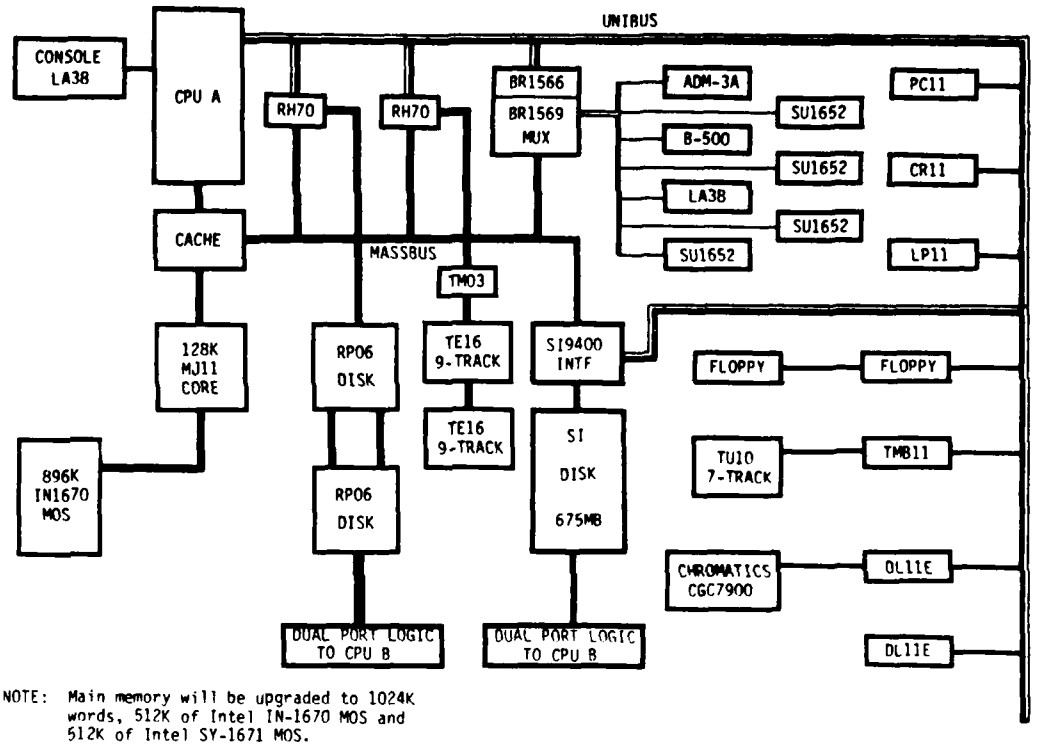
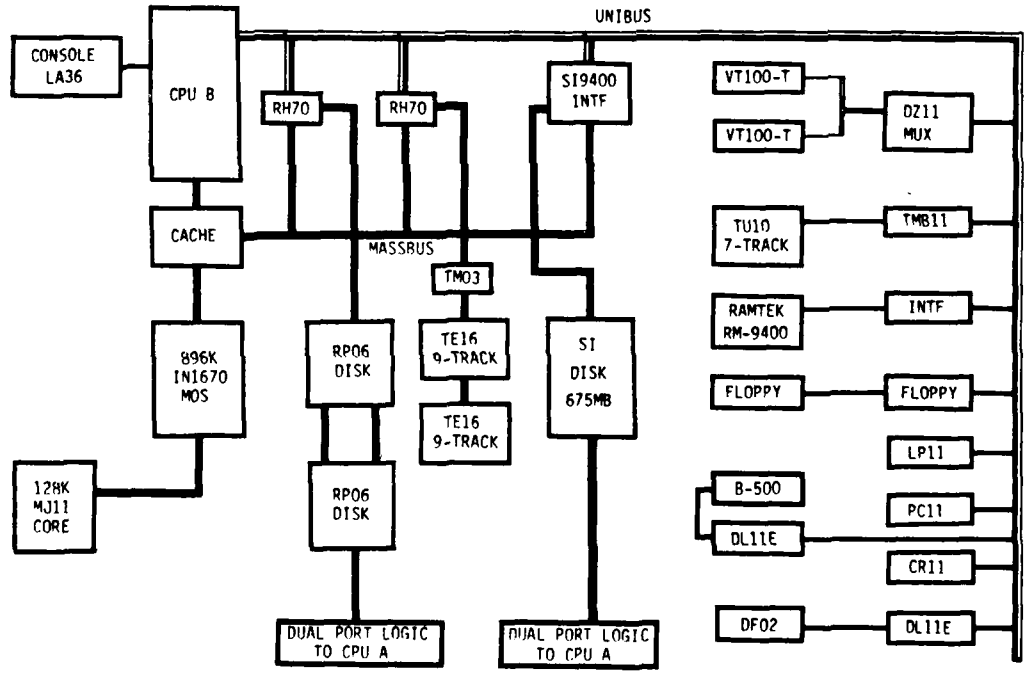


Figure 2-1. TOAS FACILITY HARDWARE CONFIGURATION



NOTE: Main memory will be upgraded to 1024K words, 512K of Intel IN-1670 MOS and 512K of Intel SY-1671 MOS.

Figure 2-2. Computer System A



NOTE: Main memory will be upgraded to 1088K words, 64K of DEC MJ11 core, 512K of Intel IN-1670 MOS and 512K of Intel SY-1671 MOS.

Figure 2-3. Computer System B

Table 2-1 TOAS Hardware List

Manufacturer	Model	Description	Quantity
DEC			
	PDP-11/70	Computer CPU, 128K core	2
	FP-11C	Floating Point Processor	2
	KW-11P	Programmable Real-time clock	2
	RWP-06BA	Dual Access Disk Controller	2
	RP-06	Dual Access Disk Drive	2
	TWE-16EA	9 Track Tape Controller/Drive	2
	TE-16EE	9 Track Tape Drives	2
	TME-11EA	7 Track Tape Drive	2
	LA-36	Decwriter	2
	LA-34	Decwriter IV	2
	LP-11VA	300 lpm Printer	2
	CR-11	300 cpm Card Reader	2
	PC-11	Paper Tape Punch/Reader	2
	DMC-11AR	DDCMP Micro Processor	2
	DMC-11DA	Network Link Line Unit	2
	DL-11E	Async Serial Line Interface	5
	VT100-T	TEMPEST Video Terminals	2
	DZ-11-T	8-Channel Multiplexer with Fiber Optic Interface	1
Intel			
	IN-1670	448K Words MOS Memory	2
Bunker Ramo			
	BR-1569	8 Channel Multiplexer	1
	BR-1566	Memory Bus Interface	1
Univac			
	SU-1652	Dual Screen Monitor (Graphics)	2
		*Dual Screen Monitor (Alpha)	2
Imlac			
	PDS-4	Graphic Display System	2

Table 2-1 TOAS Hardware List (cont.)

Manufacturer	Model	Description	Quantity
Chromatics	CGC 7900	Graphic Display System	1
Data Systems	DSD 210	Dual Floppy Disk Drives	2
Beehive Int'l	B500	Video Terminal	2
Summagraphics		ID Data Tablet/Digitizer	2
Conrac Monitors	SNA 15	15 Inch CRT Monitor	2
Genesco	CGT-3000	Graphic Display Processor	1
*System Industries			
	SI-9400	Disk Controller	1
	SI-9775	Disk Drive	1
*Ramtek	RM-9400	Graphic Display System	1

* This equipment is currently on loan to the Facility.

2.1.2 Memory

The TOAS computer system memories consist of factory installed DEC MJ11-A magnetic core memory and add-on Intel IN-1670 semi-conductor memory. Each computer system memory consists of 64K words of MJ11-A core and 448K words of IN-1670 MOS. The two memories are accessed via the Main Memory Bus or Massbus, with the MJ11 core occupying the lower addresses (0 - 400,000) and the add-on IN-1670 occupying the upper addresses (400,000 - 4,000,000). The memory configuration in System B was successfully optimized by changing the relative addresses of core and MOS memory which resulted in faster over all task execution times. Procedures used to accomplish this result are documented in Appendix A.

2.1.3 Magnetic Media Peripherals

Magnetic media peripherals of the removable media type are a means of off-line permanent data storage. This group of peripherals include disk drives, magnetic tape drives, and floppy disk drives. High data transfer rate peripherals interface to the Massbus and communicate with the CPU over the Unibus while lower transfer rate peripherals interface and communicate over the Unibus. The TOAS Facility uses a combination of DEC and Non-DEC peripherals.

2.1.3.1 RP06 Disk Subsystem

The RP06 disk drive is a high speed, moving head, removable media storage device (unformatted capacity of 176 MB) designed to operate on-line with the PDP-11/70. Features include throughput of 806K bytes per second, dual access options that accommodate manual and CPU switching between controllers, and 30 mS average seek time. The RP06 is interfaced to the PDP 11/70 via the RH-70 Massbus controller.

2.1.3.2 TWE16/TME11-EA Magnetic Tape System

Magtape transports provide the TOAS Facility with mass, off-line data storage capabilities. The TWE16 is an industry-compatible 9 track magnetic tape transport system. The unit comprises a master transport with interface and control logic, and a TE16-EA slave transport. The master transport interfaces to Main memory through a RH-70 Massbus controller.

The TE16 is capable of reading and writing magnetic tape at 1600 bits per inch in Phase Encoding (PE) mode and 800 bits/inch in NRZ mode. Tape density and character format are program selectable.

The TME11-EA is a 9 track tape system (TMB11/TE10) mechanically modified to a 7 track format. The TMB11 controller interfaces the Unibus to one TE10 tape drive. Each computer system supports one TME11-EA. The TE10 has a read/write capability of 800 bits per inch in NRZ mode.

2.1.4. Hard Copy Peripherals

Hard copy peripherals provide Facility users with program listings and permanent non-magnetic media data storage. Multi-part line printer paper is available for long listings requiring more than one copy.

2.1.4.1 LP11/LP05 Line Printer

The LP05 free standing line printer is capable of hard copy output or multicopy output on multipart forms at 300 lines/minute with 132 columns and a 64 character print drum. The LP11-VA controller interfaces the LP05 to the Unibus. Output to the printer may be either program listings or text files processed by the DEC utility Runoff.

2.1.4.2 CR11 Card Reader

The CR11 is a 285 card/minute, standard 12-row, 80 column card reader with a hopper capacity of 550 cards. The cards are stacked in the output hopper in the same order as input. The reading cycle is under external program control for single cycle or continuous run. The CR11 allows for off-line data and program storage capabilities. This device is not used at the Facility but is available if required.

2.1.4.3 PC11 Paper Tape Reader/Punch

The PC11 Reader/Punch and controller comprise a PC05 high-speed reader/punch and a PC11 controller capable of reading 8-hole tape at 300 characters /second and punching at 50 characters/second. The PC05 punch allows for off-line data and program storage capabilities. Like the CR-11, this device is available at the TOAS Facility if required.

2.1.5 User Interfaces Devices

The TOAS Facility supports several hardcopy and video user terminals. These terminals include the LA36, PDS-4/L, SU1652 and the recently acquired B500, LA38 and VT100's. LA36 system consoles allow direct manipulation of system functions and system configuration. The PDS-4/L is a stand-alone terminal that can be down-line loaded for use as a timesharing terminal, and the SU-1652M is a dedicated terminal supported by System A.

2.1.5.1 LA36 DECwriter

The Digital LA36 DECwriter is an interactive data communications terminal for use as a system console terminal. Hardware features include impact printer hardcopy output on variable width line printer paper, and a standard ASCII keyboard. The keyboard options include variable baud rates (110, 150, and 300 baud), cap locks, numeric keypad, and a line/local setting. Throughput is 30 characters/second via a 20 mA current loop DL11 asynchronous serial interface.

2.1.5.2 SU-1652M Dual Screen Monitor

The 1652 is a 15 inch dual screen micro-programmable terminal used to manually prepare, display, edit, and enter data/control signals to the PDP-11/70 via the BR1569 Communications Control Unit. In addition, the 1652 supports alphanumeric and/or graphic displays sent from the PDP-11/70.

The terminal is configured with a light pen, dual pads of variable function keys (60 keys), and interactive graphics options (joy stick). The Intel 8080 microprocessor provides terminal intelligence for remote processing. Down-line loading of complete programs is attained via the Program Load Module (PLM).

2.1.5.3 Imlac PDS-4/L Graphics Display System

The PDS-4/L in conjunction with the Pertec D3442 disk drive is a stand-alone, refreshed-graphics random stroke writer, interactive display system. Features include: a Display processor that is programmed in its own assembly language for generating displays; a Main processor for file I/O, field calculations, and other support functions. Hardware features

include: a programmable asynchronous interface (75 - 19.2K baud), 67 key programmable alphanumeric keyboard, rapid refresh display (40/second), a random deflection 21-inch CRT, and complementary software. The Pertec disk drive supplies 10 Mbytes of mass rapid access memory. In addition, the PDS-4/L is utilized as a word processor with text output sent to a Xerox 1750 printer.

2.1.6 Hardware Controllers/Interface Devices

The PDP-11/70 supports two types of communications controllers. The RH70 Massbus controller interfaces high-speed peripherals such as disk and magtape. There are also slower Unibus DMA interfaces for peripherals such as floppy disks and host driven graphics generators. The PDP-11/70 supports up to four RH-70 Massbus controllers or similar high performance controllers.

An interface serves as the communications link between the computer and other devices. Interfaces serve to translate signals sent from one device into signals that the receiving device can interpret. Most interfaces serve to electrically link I/O terminals to the computer.

2.1.6.1 RH-70 Massbus Controller

The RH-70 is the Massbus I/O controller interfaced to Cache memory for data transfers and the Unibus for control signal transfer. Major functions of the RH-70 include: communications with Main memory via Cache in order to store and fetch large amounts of data; communications with the CPU via the Unibus to receive commands, provide error and status information, and to generate interrupts; and interface with one to eight compatible mass storage disk drives via the Massbus.

2.1.6.2 BR-1566/BR-1569 Controller/Multiplexer

The BR-1566 is a high-speed Massbus interface similar to the RH-70 and occupies the RH-70 #C slots in computer system A. This device is used in conjunction with the BR-1569 Communications Control Unit (CCU). The CCU is a 32 channel I/O multiplexer designed to interface a variety of local serial and remote peripherals to the PDP-11/70 via the BR-1566. The BR-1566 can interface up to four BR-1569 CCUs.

The TOAS Facility supports a BR Controller/Multiplexer on computer System A. The BR-1569 supports the necessary hardware to realize eight active channels designated as BM channels. The BM software channels are numbered BM0: through BM7: while the actual hardware channels are numbered J1 through J8. The BM handler is the software routine utilizing the SU CRC protocol that sevices BM channels one, three, five, and seven while the TYCRT handler services BM channels two, four, six, and eight.

Available protocols on the 8 active channels are given below.

Channel	Protocol	Baud Rate
J1-BM:0	SU-CRC	9600
J2-BM:1	Interactive TTY	9600
J3-BM:2	SU-CRC	9600
J4-BM:3	Interactive TTY	9600
J5-BM:4	SU-CRC	9600
J6-BM:5	Interactive TTY	9600
J7-BM:6	SU-CRC	9600
J8-BM:7	Interactive TTY	1200

2.1.6.3 DL11-E Asynchronous Line Interface

The DL11-E is an asynchronous serial line character-buffered data communications interface designed to assemble or disassemble the serial bit stream required by data terminal I/O devices. Parallel character data can be disassembled sent serially to be reassembled at the receiving terminal and vice versa.

The unit consists of a single quad module that can be mounted in either a Small Peripheral Controller (SPC) slot or in one of the DD11-DK Peripheral Mounting Panel slots. The RS232-C protocol is implemented in data format that consist of a start bit, five to eight data bits, one odd or even parity bit or no parity bit, and one, one and one-half, or two stop bits. The baud rate is variable from 200 to 9600 baud.

2.1.6.4 DMC11 Network Microprocessor

The DMC11 network is a high performance interconnection that links two Unibus computers for intercommunications between processors. Communications between computers is accomplished by a DMC-AR/AL microprocessor module that processes and executes commands sent from the local processor

to the remote processor, or from the remote processor to the local processor. A DMC-AR/AL microprocessor module is required in each processor in the communications network. DMC11 communications format utilizes the DDCMP protocol. The DMC11 software is completely isolated from the host processor software with software communications implemented through hardware status and control registers.

Data transmission is locally implemented via coaxial or triaxial cable in half or full duplex mode. Local processor to processor data transfer rates are available at 56K-bits/second. Remote data communications can be implemented by synchronous modems and common carrier facilities, with transfer rates at 19.2K-bits/second (CCITT V.35/DDS compatible).

2.2 NEW HARDWARE DESCRIPTIONS

The major features of new hardware additions integrated into the TOAS Facility computer systems since the last reporting period are documented for ready reference and to aid in comprehending the technical aspects of this new hardware. The sub-sections detailing the Chromatics CGC-7900 color terminal and the VT-100-T fiber optics should be of particular interest to Intelligence Data Handling System sites. Section 4 also details the System Industries 9775 (Winchester) disk drive (675 MB of storage).

2.2.1 DSD 210 Diskette Memory System

Data Systems DSD 210 dual floppy disk memory system is a random access, mass storage subsystem utilizing two eight-inch single sided, single density, soft sectored floppy disks. This system interfaces to the PDP-11/70 via a SPC quad board placed in either the CPU cabinet or BA11 expander box. All data transfers between the PDP-11/70 and the DSD 210 are buffered in a 128 byte RAM. Data from the CPU is written to the RAM buffer where the data is then transferred to diskette. The CPU to RAM transfer is much faster than the RAM to diskette transfer.

The floppy disk system is shown in Figure 2-4. A formatted diskette contains 493 blocks (252K-bytes) of available storage space. This floppy disk system affords a fast and convenient method for the transfer of files between computer systems.

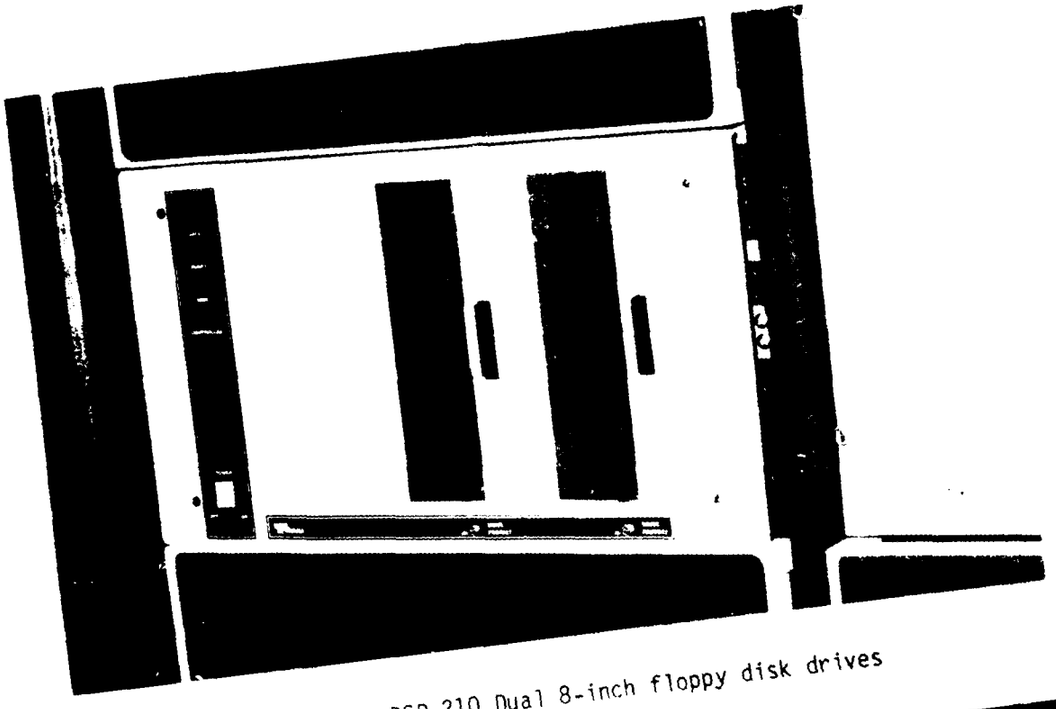


Figure 2-4. DSD 210 Dual 8-inch floppy disk drives

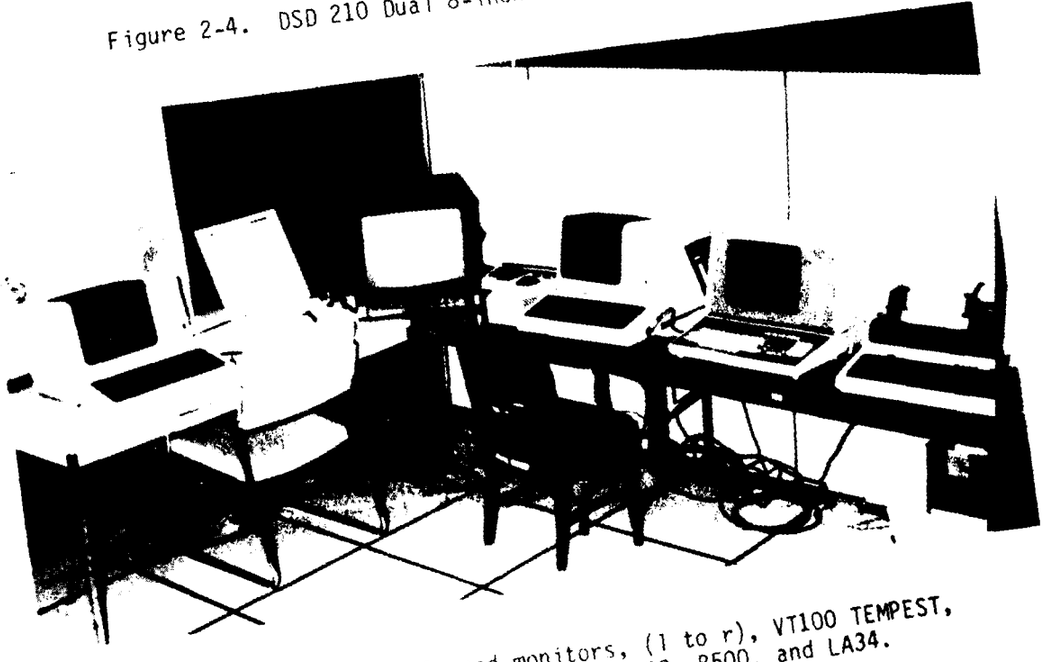


Figure 2-5. Terminals and monitors, (l to r), VT100 TEMPEST, Ramtek 9400 monitor, VT100, B500, and LA34.

2.2.2 Beehive International B500 Video Terminal

The B500 video terminal is a self-contained programmable display device incorporating an Intel 8080A microprocessor, a two page (4K-byte) display memory, and an expandable program memory. Operation may be in local text editing mode, or on-line mode over a RS-232C serial interface at speeds up to 19.2K bps.

Two basic units comprise the terminal system; a detachable keyboard assembly and a CRT monitor assembly (see Figure 2-5). Other features include: 5x7 dot matrix characters at 25 lines x 80 characters, scroll up and down within a two page display memory (40 total lines in local mode) addressable cursor, keystroke programming, and composite video output.

2.2.3 Genisco CGT-3000 Graphics Display Generator

The CGT-3000 is a host driven programmable computer graphic raster scan display system. Basic system configuration consists of a 16-bit parallel DMA interface from the CGT-3000 to the PDP-11/70. Data and instructions are passed from the host to a programmable graphics processor that processes the information into a useable display and writes this information to the memory refresh planes. A video controller and monitor controller translate the information stored in the refresh memory planes into a video signal suitable to drive a CRT.

2.2.3.1 Programmable Graphics Processor

The programmable graphic processor (PGP) communicates bidirectionally with the host computer and routes the display data between graphic memory and host computer memory. The PGP is also a programmable microprocessor capable of storing and executing programs. Processor cycle time is 150nS at two to four cycle times per instruction, with 55 instructions. PGP instruction memory is 256 16-bit words of RAM plus 4K x 16-bit words of buffer memory. Microprograms are stored/fetched in the 256x1-word RAM and calculations are performed by an arithmetic logic unit (ALU). The PGP writes data to the memory refresh planes and will alter that data upon command from the host CPU. The graphics interface portion of the PGP provides interfacing to the memory planes, video control, and monitor control.

2.2.3.2 Video Control - Monitor Control - Memory Planes

All master timing signals for the refresh memory planes and the CRT sync signals are generated and controlled by video control.

Monitor Control generates Video data to drive either color or B&W 512 x 512 video monitors at a 30 Hz refresh rate. Logic contained in the monitor control processes video data from refresh memory, cursor, and RS-170 composite sync signals. Monitor control receives single pixel data from up to eight memory refresh planes. MOS RAM memory refresh planes are utilized in a 512 x 512 resolution producing 32 16-bit words per line. The TOAS CGT-3000 contains two memory refresh planes out of a possible 16.

A 256 entry video look-up table having an 8-bit address (eight memory planes) and a 12-bit entry word (4-bits R, 4-bits G, 4-bits B) are used to define pixel color information. A pixel defined by an entry in the video look-up table (12-bit word) is gated into three 4-bit DACs for color at a given pixel. Three colors at 16 intensities create a palette of 4096 colors out of which 256 are displayable. Black and white output from monitor control is derived from the 4-bit inputs of the Red and Blue DACs. These eight input lines are gated to an 8-bit DAC to produce a 256 grey level output. The TOAS does not have a color monitor to support the CGT-3000 color capability.

The TOAS CGT-3000 contains two memory refresh planes which allows 16 grey shades or 4096 discrete colors with any four displayable (two video look-up table address bits for two memory planes for four possible addresses). Memory refresh plane operating modes include cursor tracking, incremental vectors, point to point vectors, cartesian coordinates, x-y raster, alphanumerics. Submodes include reverse write, fill cartesian, and long/short dash vectors.

2.2.4 Conrac SNA/17 B&W Video Monitor

The Conrac SNA/17 is a 17-inch diagonal, monochrome, solid state monitor designed for continuous operation at a minimum of 800 TV lines center resolution, and is capable of displaying standard 625 horizontal scan lines. This unit may be operated either from a composite video and

sync line or from seperate video and mixed sync lines. A loop-through feature allows monitor chaining. Two Conrac monitors are in operation at the Facility as slave monitors driven by CRT terminals.

2.2.5 Summagraphics ID Data Tablet/Digitizer

The Summagraphics Intelligent Digitizer will input graphics materials such as maps, diagrams, patterns, etc., in the form of binary or BCD code to a computer or data storage/retrieval device. Input to the host device such as disk, magtape, paper tape, or card punch is via a special interface or DL11-E interface with appropriate software.

Microprocessor control (Intel 8080) allows computing capability which yields high linearity and resoloution (200 lines/inch) on a 17-inch square tablet. Microprocessor control implements operational features such as binary to BCD conversion, relocatable origin, output data formatting, and computational functions such as calculating volumes, areas, linear displacements, and perimeters.

A stylus incorporating a ball point tip has a built in pressure sensitive switch actuated by pressing the ball point against the tablet to begin digitizing in point or stream mode. Digitizing an image may be accomplished in point to point mode where various points are input, or in stream mode for continuous line input at 100 conversions per second maximum.

2.2.6 LA-34 Decwriter IV

The LA-34 (Figure 2-5) is a microprocessor driven hardcopy table top terminal capable of output at 30 characters/second. The printing mechanism features a 7x9 dot matrix impact print head and is capable of printing on plain tractor fed paper or preprinted forms in rolls or fanfolds. A non-detachable typewriter style keyboard contains the full Ascii upper/lower case character set.

Other features include variable vertical pitch (lines per inch), and variable horizontal pitch (characters per inch). Communications with the host CPU are full duplex serial asynchronous transmission format utilizing an EIA RS232-C or 20mA current loop interface.

2.2.7 Xerox 1750 Printer

The Xerox 1750 (Diablo 1650 RO Figure 2-6) is a letter quality daisy wheel printer driven by any device capable of data output in an asynchronous serial format conforming to the RS232-C protocol. In its current configuration, the Xerox 1750 can receive characters at rates from 10cps to 120cps and output at 45 cps. To increase system throughput, the incoming characters are buffered in a 256 byte character buffer at a data transfer rate higher than the print rate. Status condition flags are used to halt data transfer from the host by implementing a printer ready signal which is sent to the host over pin-5 (clear to send) of the RS232 interface. When the status condition flag is cleared, the printer ready flag is again raised.

Standard status sensors include input buffer full, paper out, ribbon out, cover open, and parity error. Other features include self test diagnostics, bi-directional paper feed and carriage movement, adjustable forms width, margin control, and variable column spacing (130 or 155).

The Xerox 1750 printer is currently used as a hardcopy device for the Imlac PDS/4 terminals, the CGC 7900 display terminal, and also on BM:7 of the Bunker Ramo 1659 Multiplexer. The DEC utility, Runoff, is currently employed to output Files-11 text files from the PDP-11/70 to the 1750 via the BR 1569 multiplexer.

2.2.8 DF02 Modem

The DF02 Modem (DEC) is a communications device that converts remotely generated modem audio tones (analog signals) into digital signals electrically compatible with the DL11-E interface. The remote audio tones are sent to the DF02 modem via public telephone at 300bps and are routed to a processor through a DL11E PDP-11/70 interface. A standard Bell System telephone set is used to automatically answer calls after the third ring. Currently the DF02 modem is generated into the TOAS System B (time-sharing). To communicate with the TOAS computers, the remote user dials in over a dedicated line, where after three rings of the telephone to which the DF02 is linked, the modem detects an audio carrier present, verifies

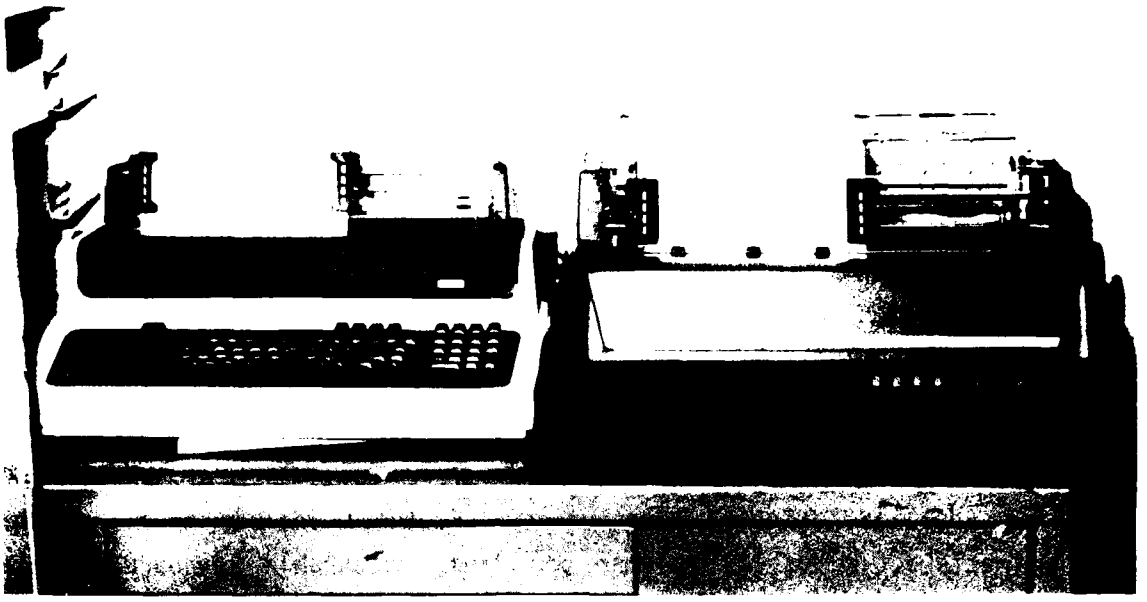


Figure 2-6. LA 34 Decwriter IV (1), and Xerox 1750 word processor.

Figure 2-7. VT100-T TEMPEST terminal with fiber optic interface.

that the data terminal is ready to receive, and verifies that the transmission line is ready for use. At this point, the communications link has been established and is ready without any operator intervention.

The DF02 modem can also be implemented as a remote modem. A TOAS user can connect a terminal to the DF02 and dial into any other remote processor that has a modem electrically compatible with the DF02.

2.2.9 VT-100-T Video Terminal (TEMPEST Approved)

DEC's VT-100-T shown in Figure 2-7 is a TEMPEST modified version of the VT-100 video terminal and includes most functions of the VT-100 including identical internal electronics. Features include double width/size characters, up to 132 columns per line, detachable keyboard, smooth scrolling, split screen, and power-up self test diagnostics.

An internal terminal controller manages all displays and communications utilizing an Intel 8080 microprocessor. Functional components of the terminal controller include a video processor for data to video conversions, 3.072K bytes of RAM for screen data storage and a micro scratch memory. Micro instructions are stored in 8.192K bytes of ROM and user alterable features such as tabs, baud rate, type of cursor, reverse video, etc. are stored in nonvolatile RAM (NVR). Communication with a host processor is via a UART (75-19.2K bps) in full duplex mode. An advanced video option board expands the CRT display from 14 to 24 lines and also extends character attributes.

To meet the TEMPEST requirements for electromagnetic emanations suppression from data transmission lines, the VT-100-T utilizes the EIA to fiber optics adaptor shown in Figure 2-8. Fiber optic transmission lines do not generate any electromagnetic fields and are therefore free of any electromagnetic emanations. This terminal is interfaced to the PDP-11/70 through a DZ11-T 8-line asynchronous multiplexer where the multiplexer inputs have been modified to accept fiber optic inputs. The MIL STD 188C interface is also available in addition to the fiber optics interface and also meets TEMPEST requirments.

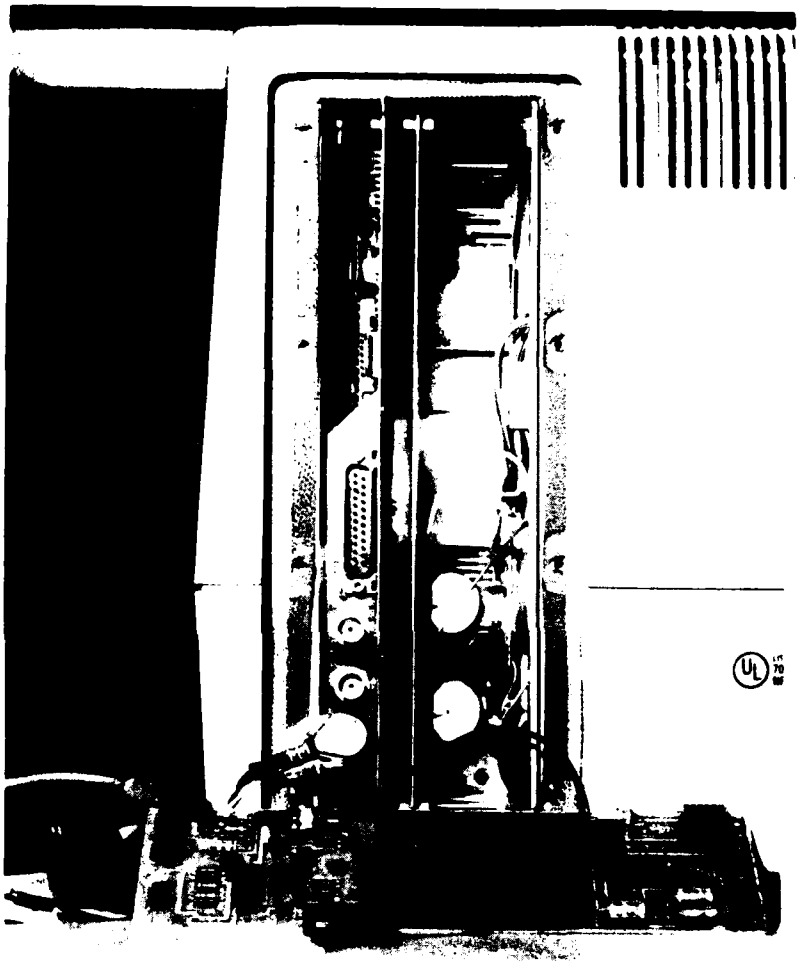


Figure 2-8. Rear view of VT100 fiber optic interface board.

2.2.10 DZ11-T 8-Line Asynchronous Multiplexer

The DZ11-T is an 8-line asynchronous multiplexer supporting an interface that translates fiber optic input signals to the RS232C protocol. This fiber optics to EIA RS232C translation is necessary to support the fiber optic outputs from the VT-100-T video terminal. The DZ11 meets the electromagnetic emanations suppression requirements of TEMPEST.

Each channel may be separately configured for data format and transfer rates of up to 9600 bps in full duplex mode. The terminal handler software polls each data channel and responds on a first come first served basis. Each DZ11 may be expanded to 16 channels by adding channels in groups of eight.

2.2.11 Chromatics CGC-7900

The CGC-7900 is a color graphics terminal capable of displaying graphics sent from a host CPU or graphics that have been interactively created in stand alone mode and internally stored. Graphic displays are easily created in a stand alone interactive mode and stored on either a 10 Mbyte Winchester disk or on two double density floppy disk drives. The complete stand alone unit is shown in Figure 2-9.

All graphics creating functions translate into a string of ASCII characters which are stored on disk media. The ASCII command string may be recalled and executed which results in the redrawing of the stored display. This method of storing only graphics command strings enable more displays to reside on a given storage medium rather than attempting to store an entire bit map display.

2.2.11.1 System Features

System features include a 16-bit microprocessor (Motorola MC68000) CPU, 10 Mbyte Winchester disk drive, dual double density floppy disks, and a high resolution raster scan 19-inch color CRT having 1024x768 viewable pixels at a 60 Hz refresh rate. Also included is a 151 key keyboard having the full ASCII character set, 24 programmable function key strokes, and eight programmable bezel keys located below the CRT face.

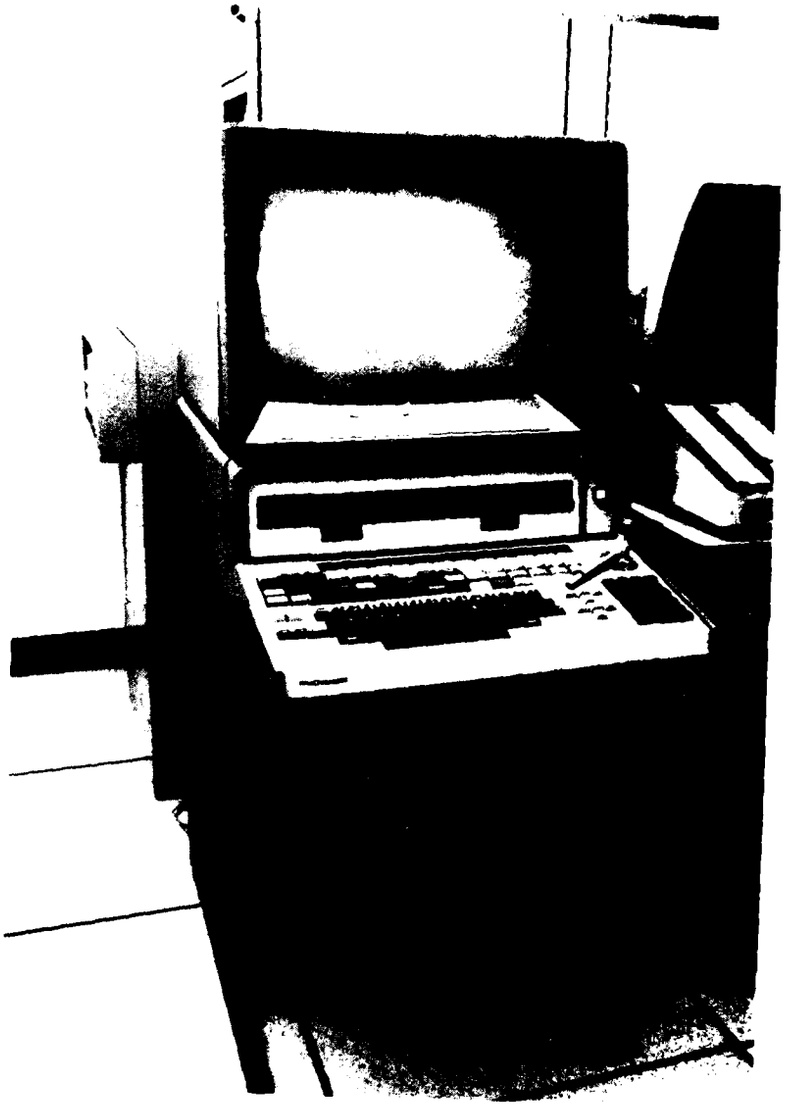


Figure 2-9. Chromatics CGC 7900 color graphics display system.

Basic display building geometric patterns are available as a simple sequence of keyboard key strokes. For example, to draw a circle the user depresses the 'circle' key then enters the center coordinates and a radius. Drawing a triangle consists of depressing the 'triangle' key and entering three vertex points. Arcs, polygons, vectors, and other display characters follow a similar drawing method. Coordinate points may also be entered through the joy stick cursor or light pen input. So, to display a triangle the three vertex coordinates are entered by light pen or cursor position.

2.2.11.2 Hardware Description

The MC68000 CPU executes all functions necessary for an operational system with the aid of the keyboard support processor. Upon keyboard input, the CPU will execute the proper instructions to draw a display into one or the other group of memory bit planes. Two complete graphic displays can be stored in two separate and complete groups of memory bit planes, with both groups alternately viewable.

Each display memory bit plane contains 1024x1024 addressable bits. If one group of bit planes is configured to the maximum of eight planes per group, one of 256 predetermined colors are displayable at each of the 1024x768 viewable CRT pixels. The CPU implements hardware pan and zoom that allows display of pixel information contained in bit map lines 769 to 1023, i.e. almost half of the display is not presented to the CRT at any given time. One bit plane can serve as an overlay which allows specific parts of a display to be masked or enhanced. Overlay capabilities include overlay on/off, alphanumerics of selectable size, shape, color, and variable angle character base line (characters displayable at any angle diagonally across the CRT. A software/hardware modifiable video look up table is 24-bits wide at 8-bits per primary color. Each primary has 256 intensities allowing for a diverse color palette, from which 256 colors are selected.

Currently available software for the TOAS CGC-7900 is a disk operating system (DOS 1.6), IDRS operating system, C, Pascal, and FORTRAN compilers. Also included are system hardware diagnostics on floppy disk media. In the near furture, DOS 1.6A will be released which improves hard disk file access.

2.2.12 Ramtek RM-9400 Graphic Display Generator

The Ramtek RM-9400 shown in Figure 2-10 is a host processor driven, raster scan color video display/generator system. This system is capable of single or multi-channel output operation and may be configurable as an output peripherial or an on-line interactive display system.

Modularized system components are selectable with a typical system configuration supporting a rack mounted RM-9400 display generator, 1024x 1024 pixel color CRT, keyboard, trackball or joystick, and an 11-inch square digitizing tablet.

2.2.12.1 Display and Memory Control Processors

Multi-bus architecture and multi-processors enable simultaneous operation of different processing elements within the system. The display generator based on the Z80 microprocessor handles programmed I/O (PIO) and direct memory access (DMA) transfers via 16-bit parallel interface. It controls or indirectly controls each element of the display system.

The memory control processor draws alphanumerics, graphics, images, etc. into refresh memory. Memory control is a 16-bit special purpose microprocessor with dedicated ROM, RAM, and support logic which can perform window clipping and pan/zoom functions.

2.2.12.3 Refresh Memory and Video Generator

Refresh Memory consists of MOS RAM arranged in a 1024 x 1024 bit dot matrix format that stores displays written to it by the display processor. This format is processed by the Video Generator which outputs a standard composite video signal suitable for CRT display.

2.2.12.4 Software and Options

FORTRAN libraries available from Ramtek serve as general building blocks for display building. Several interfaces and device handlers for popular minicomputers and operating systems are also available. Users may down-line load display processor code that will augment or redefine the standard instruction set and implement local application oriented functions. Ramtek self-booting tape diagnostics are also available.

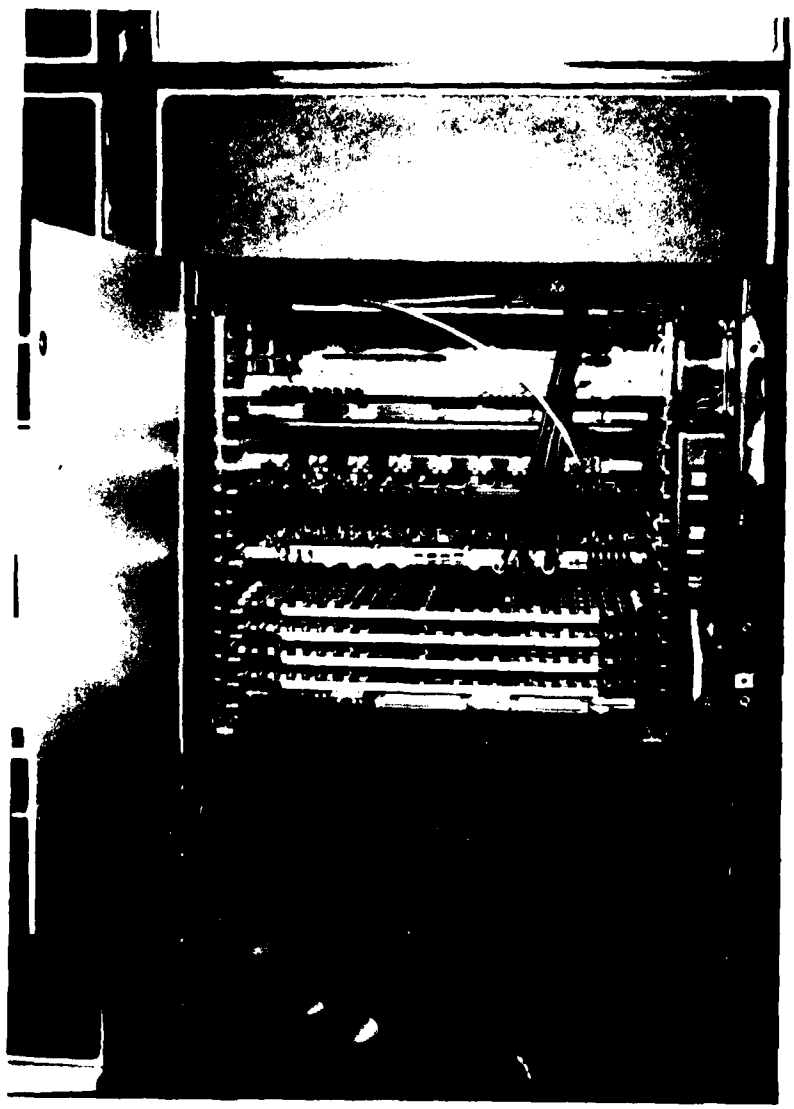


Figure 2-10. Ramtek RM-9400 color graphics display processor in rack mount.

From one to eight system peripherals such as keyboards and track balls may be interfaced to the system through an optional serial link board. Support software is available for keyboards, trackballs, joy sticks, light-pens, and digitizer tablets. The TOAS RM9400 system contains a type II video generator for general image processing and sophisticated graphics.

2.3 SOFTWARE TECHNICAL DESCRIPTION

This section provides a description of newly acquired software, software under consideration, and the baseline software available at the TOAS Facility. This description will include operating systems, data base management systems, graphics packages, languages, and utility programs.

2.3.1 New Software

The TOAS Facility attempts to acquire new software as it becomes available. Two new pieces of software have been acquired; the first is the General Purpose Interactive Display System (GIDS) and the second is the relational Data Base Management System ORACLE. Other software that is under consideration is also described in this section.

2.3.1.1 A Relational Data Base Management System - ORACLE

ORACLE was installed at the TOAS Facility on 21 July 1981. The documentation and support provided by RSI allowed a smooth, fast software installation and integration at the TOAS Facility. The relational data base model implemented by ORACLE is well suited for use on Project 2315 and elsewhere in the intelligence community due to the increased speed (query dependent) and versatility over more traditional data base models. ORACLE is capable of searching large tables of data at very rapid rates. Search times can be favorably reduced by carefully building tables and selecting indexed fields. Several tables have been loaded at the TOAS Facility for benchmark testing and demonstration purposes. The type of data, number of records, and length of records are indicated below.

TYPE	# OF RECORDS	RECORD LENGTH (BYTES)
EOB(Installation Data)	1638	512
EOB(Radar Site Data)	3201	448
AIF	16850	640
IROF	9544	906

ORACLE can be called from applications programs or can be used interactively to support ad hoc queries. This flexibility, when combined with large amounts of intelligence data, provides a solution to data management problems. ORACLE provides all of the features necessary for data security and data recovery. If a data base is defined as secure, that data base's dictionary contains information about the users of the data base in addition to a description of data stored within the data base. This allows ORACLE to control access to the data base by a user on an access privilege basis.

- DEFINE USER - The creator of a secure data base can authorize additional users by means of this command.
- User Name and Password - A secure data base requires an authorized user to supply his predefined User Name and his Password.
- GRANT Privilege - This command allows users to control access to their data by other users. Once granted, these privileges may be rescinded by using the REVOKE command.

Data recovery is almost as important as data security; therefore, ORACLE provides a complete journaling utility. The following journal (JNL) commands are available:

- JNL START - starts the ORACLE journal (if journaling is to be used, this should be part of the start up procedure).
- JNL STOP - stops the ORACLE journal.
- JNL DBSTART - starts journal activity for a particular data base. Once this command is given, journal activity will begin in future sessions unless specifically instructed to stop (see JNL DBSTOP).
- JNL DBSTOP - stops journal activity until restarted.
- JNL APPLY - used to recover a data base by applying the journal to the last saved copy of the data base.
- JNL STATUS - used to display the journal activity within the ORACLE environment.

The only data base not journaled is the ORACLE system data base. If a failure occurs on it, the Data base File Utility (DBF) must be used to recreate the system data base and enter the user data bases. Journaling is an absloute necessity in maintaining data integrity.

2.3.1.2 General Purpose Interactive Display System (GIDS)

GIDS is an IR&D project sponsored by TRW Defense & Space Systems Group. GIDS was developed to provide a device independent graphics system. This goal is accomplished by using hardware dependent display drivers and a universal display language.

The design concepts of GIDS are firmly based on accepted programming techniques. Since graphics display technology is rapidly changing, the need to write transportable applications software is emphasized. By using a universal display language and display drivers, applications software can be transported from one hardware system to another without modification. Thus "throw away" software is kept to a minimum. GIDS is an exceptionally flexible man-machine interface (MMI) evaluation tool. GIDS can be used on the IMLAC and the Ramtek 9400 display devices. A device driver to support the CGC 7900 will be available at the TOAS Facility soon.

The GIDS Executive was designed to support the addition of new functional capabilities with minimal impact on overall system operations. The GIDS architecture provides for functional expansion on three levels:

- The development of additional device drivers for adding new display devices to the system.
- The development of additional functional display elements.
- The development of special user oriented man-machine interface modules.

The GIDS system consists of six display processors. The six are:

- Briefing Processor - used to display flow, network, or any symbol oriented diagrams using standard flow charting symbols.
- Graph Plotting Processor - used to display statistical data in pictorial form.
- Geographic Processor - used to:
  - Display charts showing land masses and political boundaries
  - Define a time window
  - Display platform movement histories
  - Display platform location characteristics
  - Display tactical situations
  - Calculate distances, travel times, and routes

- Geographic Overlay Processor - used to:
  - Develop command and control scenarios and simulations
  - Display platform movement histories and the current location of platforms of interest
  - Perform intelligence gathering functions
  - Display tactical/potential combatant situations.

- Analysis Processor - used to perform calculations on user supplied information, i.e., "What is the travel time, course, and distance between two points on the Earth's surface?"

- Status Processor - used to display the contents of a file and to create one or more lines of text.

2.3.1.3 DI-3000

DI-3000 is a graphics software package that is commercially available from Precision Visuals, Inc. It has been implemented in 1966 ANSI FORTRAN as a library of FORTRAN callable subroutines. The design of DI-3000 is based upon the fundamental premise that computer graphics programs should be device independent. Through true device independence, an applications program will produce similar or even identical images on several different graphics devices. To achieve device independence, DI-3000 targets all graphics output commands and input requests to a virtual graphics device. A device driver is then used to translate virtual graphics device commands into device dependent commands. A device driver is a library of subroutines that interpret the device independent commands generated by the device independent routines, and converts these commands into the device dependent instructions required to drive specific graphics devices.

Some outstanding features of the DI-3000 graphics software package that are noteworthy include:

- An application program may reference one or more virtual graphics devices. At run time there will be a one-to-one correspondence between the active virtual graphics devices and the active device drivers.

- For each physical display device there is a corresponding device driver. The device driver translates device independent commands into device dependent instructions. The device driver will always try to implement commands through the device's hardware or firmware first. If not possible, it will try to simulate it using software. If this fails, the command will be ignored.

- DI-3000 was modeled after a proposed graphics standard; therefore, it utilizes a world coordinate system which can be either two dimensional or three dimensional. This world coordinate system is used to define the orientation of primitives (e.g., moves, lines, characters, special symbols).

- Application programs define the mapping from a window in the world coordinate system to a viewport in the virtual coordinate system. This mapping is called a viewing transformation.

- Facilities are provided for applications programs to perform scaling, rotation, translation, and shearing.

- The DI-3000 metafile is a sequential file of pictures generated by a DI-3000 program. The metafile is in essence a "picture audit trail". Whenever a new picture is created, it will be written to device 0 (the metafile) simultaneously with being written to the user selected graphics device. By using the metafile translator, these pictures may be positioned, scaled, and superimposed on a selected graphics device.

DI-3000 has been designed as a modular software network. Through this modularity and a network manager, device independence can be insured (see Figure 2-11). The application program can only communicate through the DI-3000 device independent routines. These routines in turn communicate with the network manager. Through the network manager, the application program is then indirectly linked to the metafile processing system, the device drivers, and the segment storage area.

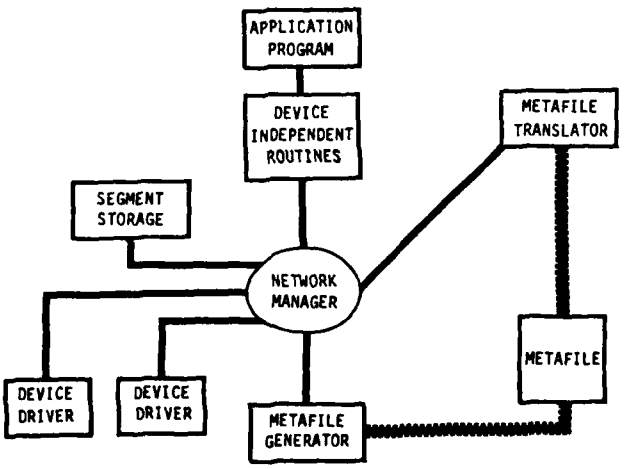


FIGURE 2-11. DI-3000 Organization

DI-3000 also provides much flexibility in the appearance of the display through the use of selectable display attributes. The attributes for non-text primitives include:

- Color
- Intensity
- Linestyle (e.g., solid, dashed, or dotted)
- Pen (represents a compostion of color, intensity, linestyle, and linewidth)
- Polygon Edge Style
- Polygon Interior Style
- Polygon Interior Color and Intensity
- Marker Symbol (index number of symbol to be displayed)

DI-3000 also provides a set of attributes for text. These are:

- Character Path - *determines the direction of the text*
- Character Font - defines the typeface (e.g., simplex, complex, or italics)
- Character Justification (e.g., left, center, or right)
- Character Size
- Character Gap - determines intercharacter spacing
- Character Base - defines the orientation of the baseline of a string of characters in the world coordinate system.
- Character Plane - defines a plane in the world coordinate system in which characters will lie.

2.3.1.4 A Real-time Multi-programming System - RSX-11M

RSX-11M is Digital Equipment Corporation's (DEC) primary real-time operating system for PDP-11 systems. RSX-11M will support multi-tasking, dynamic memory management, multiple programming languages, interactive program development, and a variety of device interfaces. It will run on any PDP-11 processor excluding the LSI-11. The minimum system

configuration requires a console terminal and either one of the larger disk systems plus a magnetic tape system or an RK05 disk system with a secondary storage device (e.g., DECTape or "Floppy" Disk). Using a PDP-11/70 processor with memory management hardware, 4M bytes of memory are addressable. RSX-11M is designed to provide a resource-sharing environment ideal for multiple real-time activities. One of the goals of RSX-11M is to handle multiple requests for service while maintaining real-time response to each request. This is achieved partially through the following services:

- multiprogramming
- priority scheduling
- power-failure shutdown and auto-restart
- disk based operations
- checkpointing
- dynamic memory allocation (optional)

Multiprogramming in a single processor system is achieved by partitioning memory. Each task is assigned to a partition at task-build time and all partitions can operate in parallel. With a single processor, only one task can have control of the CPU at a time. If a task is not using the CPU (e.g., if it is waiting for I/O), another task which is ready to execute will be granted control of the CPU. This implementation tries to achieve maximum possible CPU utilization. In RSX-11M, user controlled partitions can be subdivided allowing a greater number of tasks to be active, thus increasing system throughput.

RSX-11M is mainly event-driven and is not strictly a time-slicing system as are many operating systems. In an event-driven system, CPU control will be granted to the highest priority task capable of executing. This task will retain control until a significant event is declared or an external interrupt occurs. A significant event occurs when a task issues a system directive that implicitly or explicitly suspends a task's execution. For example, a task can issue a directive that indicates it wants to wait

until an I/O operation is complete before continuing execution. At this point a significant event is declared. Event flags are used to indicate the status of an operation. When an event flag is set, the executive declares a significant event and the highest priority task capable of executing will gain control of the CPU. An external interrupt will also cause a task to release control of the CPU. Interrupts will occur for such things as control characters entered from the keyboard or a device error. When an interrupt occurs, the program counter will be loaded with an interrupt vector and an interrupt service routine (ISR) will be executed. After the ISR has completed, normal priority scheduling will resume.

An option available at system generation time is to choose another scheduling algorithm. RSX-11M systems allow the user to supplement event-driven task scheduling with time-based round robin task scheduling.

Power Failure Restart is the ability of a system to smooth out intermittent short-term power fluctuations without visibility to the user and without loss of data. RSX-11M accomplishes this by:

- When power begins to fail, the processor traps to the executive which stores all register contents.
- When power is restored, the executive receives control and restores the previously preserved state of the system.
- The executive then informs any tasks that have requested power failure restart notifications through the Asynchronous System Trap mechanism that a power failure has occurred. These tasks can then make any restorations of state they deem necessary.
- The executive schedules all device drivers that were active at the time the power failure occurred at their power failure entry point.

A disk based computer system uses random access peripherals both as an extension to main memory and as the primary data storage medium. This provides the base for program development facilities, a common file system, checkpointing, and rapid task initiation.

Checkpointing is an option selectable at task build time and will determine if that task can be suspended. A checkpointable task can be swapped out of memory when a higher priority task requests that memory

partition. This makes it possible to achieve maximum processor utilization. Checkpointability of a task is a factor of the tasks priority. A higher priority task requesting the partition will cause the task currently resident in the partition to be checkpointed and swapped out to disk.

Dynamic Memory Allocation allows the system to load and execute multiple tasks in a single partition. The executive will begin by loading the highest priority task into the first available block of contiguous memory large enough. The executive will continue to load a partition as long as there are contiguous blocks of memory remaining. When a task completes execution, it will release all memory allocated to it. This may lead to memory fragmentation. For this reason the dynamic memory allocation option can perform automatic memory compaction. If this option is included when a task releases a block of memory, the remaining tasks will be relocated to provide the largest contiguous block of memory possible.

2.3.1.5 UNIX

UNIX is a general-purpose, multi-user, time-sharing operating system written by Bell Telephone Laboratories, Inc. and is a registered trademark of Bell Laboratories. The first version was released in February, 1971 and was implemented on PDP-7 and -9 computers. UNIX Version 2 was released for the PDP-11/20 computer. All subsequent versions have been for the more recent PDP-11 series computers (PDP-11/40, /44, /45, /70). According to a paper presented at the Tenth Hawaii International Conference on the System Sciences in January 1977, only five years after the first release, UNIX was being used by more than 150 universities, fifteen commercial and government organizations, and at approximately 250 Bell System facilities. Its major uses include preparation and formatting of textual material, collection and processing of trouble data from Bell System switching hardware, and for computer science research in topics such as operating systems, language processors, and computer networks. One of the unusual characteristics of UNIX is that all modern versions are written in an higher-level language vice assembly language. The early versions of UNIX were written in PDP-11 asssembly language. While this reduced the size of the code and provided

for somewhat faster execution times, it made the operating system inflexible to modification. In mid-1973, UNIX was rewritten in the "C" programming language. The size of the new system is about one-third greater than the old. This increase in size is usually considered acceptable since the new version is much easier to understand and to modify and also includes many functional improvements including multiprogramming and the ability to share reentrant code among several user programs.

UNIX supports a tree-structure file system which contains three types of files: ordinary files, directories, and special files. Ordinary files contain whatever information the user places in it. Directories provide the mapping between the names of files and the files themselves. Special files are a unique set of files associated with I/O. Each I/O device supported by UNIX is associated with at least one such special file.

In a tree-structured file system the nodes can either be a directory (branch) or an individual file (leaf). Both of these types of nodes may be traced back to the top of the tree (root node). A node contains a description of the file and consists of the following items:

- its owner
- its protection bits
- the physical disk or tape address for the file contents
- its size
- time of last modification
- the number of links to the file
- a bit indicating whether the file is a directory
- a bit indicating whether the file is a special file
- a bit indicating whether the file is "large" or "small"

This information is called an "i-node" and is created whenever a new file is created. Once a file and its corresponding node are created, the node will remain in the tree so long as at least one link to the node remains. Anytime a file is accessed, a link is created. If the number of links

reaches zero, indicating the dirctory no longer is maintaining a link to the file, the node will be removed from the tree.

The system calls to do I/O are designed to eliminate the differences between the various devices and styles of access. There is no distinction between "random" and "sequential" I/O, nor is any logical record size imposed by the system. The size of an ordinary file is determined by the highest byte written on it; no predetermination of the size of a file is necessary or possible. One of the techniques used to improve run time of most programs is that the system recognizes when a program has made accesses to sequential blocks of a file and asynchronously pre-reads the next block. A comparison of I/O speeds was made by Bell Laboratories between IAS and UNIX. The test consisted of timing a program which copied a file containing 480 blocks (245,760 bytes). The execution time under IAS was 19 seconds, while the execution time under UNIX was 25 seconds; however, the following hardware differences should be noted. On the UNIX system as opposed to the IAS system, the disk drives were older. While the seek times were essentially equal, the average rotational latency was 4.2 ms. longer and the block transfer rate was 1.3 ms. longer on the UNIX system. If one corrects the UNIX time for this hardware difference, the transfer rates become essentially the same.

Operating System security is the ability to protect against unwanted accessing or destruction of data and against denial of service to others, for example by causing a crash. The weakest area is in protecting against crashing, or at least crippling the operation of the system. Early versions of UNIX (circa 1975) did not check for overconsumption of certain resources, like file space, total number of files, and number of processes. Running out of these resources will not cause a crash, but will degrade system performance to the point of unuseability. Files are adequately protected by the assignment of protection bits. There are nine protection bits broken into three groups of three bits. These control permission to read, write, and execute a program by the owner of the file, the member of the owner's group, and by all others.

Some shortcomings of UNIX include:

- UNIX is not a "real-time" system.
- There is no general inter-process message facility.
- Input and output are synchronous.
- Memory is not shared between processes, except for the read-only program text.

2.3.2 Baseline System Software

In addition to the new software previously discussed, the following baseline software is available for use at the TOAS Facility.

2.3.2.1 Interactive Application System (IAS)

IAS is DEC's general purpose operating system implemented on the PDP-11/70 processor. It is a multi-user timesharing system that supports up to 32 concurrent interactive, real time, and batch users. The TOAS Facility has IAS Version 3.0 operating in the timesharing mode; the other operating system modes (*Real-time and* Multi-user) could be generated if required.

2.3.2.2 Data Base Management System (DBMS-11)

The DBMS is an implementation of the CODASYL data base language specification. The DBMS provides data control and manipulation functions for application programs. The application programs can be written in COBOL, FORTRAN, or other languages using the CALL statment.

DBMS supports network and hierarchical type data structures and permits structure definition suitable to the applications. It also provides a separate language facility, Data Description Language (DDL), for description of the complete data base or portion of the data base. For a detailed discussion of the DBMS concept, refer to the Data Base Administrator's Guide.

2.3.2.3 DECnet-11

DECnet is a software package that extends the IAS operating system to form computer networks. The DECnet facilities provide for program

sharing and intertask communication. Peripheral devices from a remote system may be connected to a host computer system and used via DECnet. The files from the remote system may be shared or new files opened for storage.

An executable program module may be transferred to a remote system for execution (down-line loading or specific tasks). Intertask communication is allowed between two tasks, either locally or remotely.

2.3.2.4 COBOL Compiler

The COBOL compiler translates ANS-74 COBOL source into relocatable object modules. The compiler runs under the supervision of the IAS operating system and conforms to all connections and restrictions of IAS. To run a COBOL program, a five step process is required: (1) Prepare the source program. (2) Compile the source program. (3) Merge or prepare an overlay description file (optional). (4) Task-build the object modules into an executable task. (5) Execute the task. For a detailed description of COBOL use, refer to the COBOL User's Guide.

2.3.2.5 FORTRAN Compiler

The FORTRAN-IV Plus compiler is supported at the TOAS; however, FORTRAN-IV with virtual data arrays can be installed if required. For a detailed description of compiler use, compiler diagnostic messages, and the run time diagnostic messages, refer to the FORTRAN-IV Plus User's Guide. For a more detailed description of specialized applications, an Object Time System Reference Manual is provided by the Facility.

2.3.2.6 GRAPHELP

GRAPHELP is an interactive graphics FORTRAN-IV software package that runs on a PDP-11 computer system. The GRAPHELP package supports all Tektronix 401X Graphic Storage Tube Terminals and the Imlac PDS-4/L Refresh Graphics Display System. The software provides both absolute and relative vectors of four varying line textures, user definable scaling, windowing, clipping, terminal transparency, and 128 nested subpicture display files for refresh graphics. Routines are provided for interactive

graphics crosshair input and screen erase control. The applications are oriented towards data plotting for both linear and logrithmic data, along with alphabetic and numeric symbol output. The documentation for GRAPHELP is contained on the timesharing disk. The GRAPHELP libraries referred to in the documentation (PLTFTN, TKGFTN, IMGFTN, ALLFTN) are built and also located on the timesharing disk.

2.3.2.7 Program Load Module (PLM)

The Program Load Module (PLM) is a down-line loader for the SU-1652 terminal. This software was developed by Sperry Univac Corporation for the Rome Air Development Center. A copy of the object software was provided for use at the TOAS Facility by the government. The PLM software allows the user to easily update tables containing SU-1652 micro-code modules and terminal characteristics. This allows system managers to dynamically change the software characteristics of SU-1652 terminals. Complete documentation is provided at the TOAS Facility.

3. FACILITY MANAGEMENT PROCEDURES

The purpose of this section is to provide the standards and guidelines for TOAS facility operation. This section is applicable to all contractor and government personnel using the TOAS facility and is effective upon publication and distribution. This document does not supersede any existing documentation but is intended as a guideline for orderly, efficient management of the TOAS facility resources. Other applicable documents include:

- TAC-RADC Memorandum of Agreement
- ESD-TAC Host Tenant
- Project 2315 Contracts
- ASPR Series Documents

3.1 PROJECT 2315

Project 2315 is an advanced Research and Development (R&D) effort sponsored by the Rome Air Development Center (RADC/IRDE). The program is designed to develop prototype equipment, techniques, and procedures to enhance USAF tactical operational intelligence functions and supporting processes. The program also provides functional specifications, designs, alternatives, and prototype elements for follow-on systems. The TOAS Facility is the focal point for conducting demonstrations of operational intelligence functions such as collection management, targeting, etc., along with validation of concepts and functional specifications.

3.2 FACILITY OPERATIONS AND PROCEDURES

The TOAS facility is the focal point of the Project 2315 Tactical Intelligence development and other RADC sanctioned R&D efforts. Since the facility is located within an Air Force tactical operations environment, developer-user interaction is promoted, and an increase in the timeliness and appropriateness of the R&D programs engineered and managed by RADC is expected. (See Figure 3-1 for project management structure).

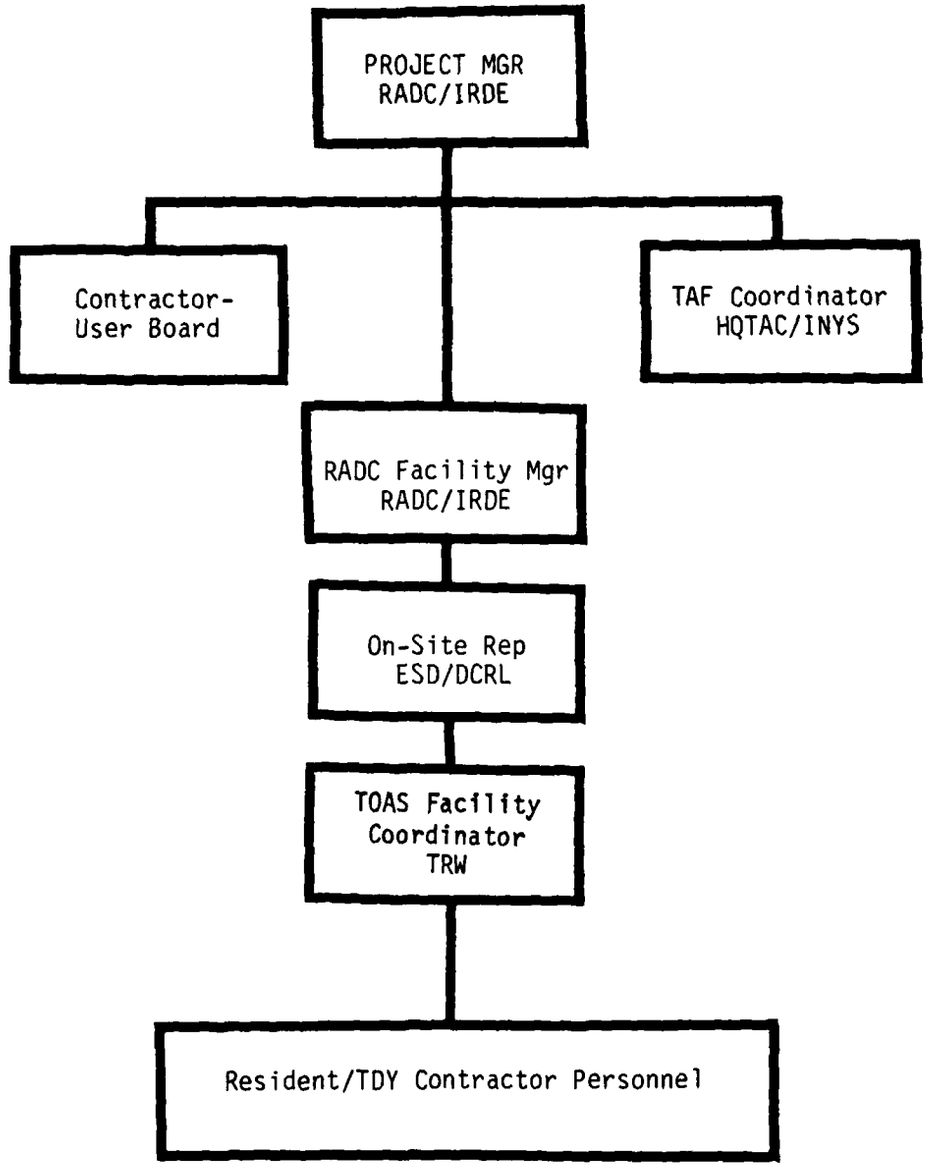


Figure 3-1. Project 2315 Management Structure

The facility, dedicated to R&D activities, provides the flexibility to change software and hardware components with minimal constraints. The daily TOAS Facility operation is the responsibility of the Facility Coordinator, while overall operation is the responsibility of RADC. A list of project-related definitions is in Appendix 3-A to this section.

3.2.1 Hours of Operation

The facility will normally be open and available for users from 0700-1700 hours five days/week. An additional 5 hours per week are used for preventive maintenance activities.

3.2.2 Security and Visitor Control

3.2.2.1 Physical Security

The TOAS facility is located in building 23 (Langley AFB, Virginia) which is approved for open storage of DOD Secret material. Unescorted entry into this building requires a Secret security clearance be filed with the 460 Reconnaissance Technical Squadron (RTS) Security Office which controls access to this building.

3.2.2.2 Visitor Control

All visit requests for purposes other than working with permanent resident contractors must be sent to:

HQ ESD/DCT
BLDG 27
LANGLEY AFB, VA 23665

ATTN: MR K. H. SHINGLER

Unescorted entry into Building 23 can not be granted unless a valid security clearance (SECRET) is on file. If required, pass sensitive compartmented information (SCI) clearances via appropriate channels to:

AFSSO TAC
PASS TO 460 RTS (ATTN: TOAS FACILITY)
LANGLEY AIR FORCE BASE, VIRGINIA 23665

3.2.2.3 Computer Security

Computer facility security will be the responsibility of the Facility Coordinator; each contractor/agency using the facility is responsible for any classified working papers generated at the TOAS Facility; proper disposal of classified material is also the responsibility of the individual contractors.

3.2.3 Physical Facility Structure

The facility is divided into an office area and the computer area. An expansion of this area is expected early in CY82 to provide for an Intelligence Functional evaluation area.

3.2.4 Computer Hardware Operations

In order to provide the maximum flexibility and benefit to TOAS Facility users, the concept of open and controlled computer system will be implemented.

3.2.4.1 Open Computer System

An "open" computer system is one that is dedicated to a single system user or dedicated to several users working together to demonstrate a single TACC task, e.g., collection management, targeting, etc. The TOAS Facility is configured with dual PDP-11/70 processors. This may be a single system user for each CPU, or a single user may have control of both CPUs. During this period the single user has direct access to all system component and peripheral devices (i.e. tape/disk drives, I/O devices, etc.). Computer operator services are provided on an as requested basis only.

3.2.4.2 Controlled (Closed) Computer System

This system is configured to support several users in a time sharing environment. User services are provided by a computer operator assigned by the Facility Coordinator. Users have complete access to tape and disk drives and system I/O devices. Support for program/file development is a typical application of this type of system configuration. The "time share" environment is normally scheduled daily.

3.2.4.3 Baseline System

The initial Project 2315 baseline will consist of the commercial hardware and software configuration items. As new software modules are developed, tested, and demonstrated, these modules may be added to the baseline with the Configuration Control Board (CCB) approval. The Facility Coordinator will store and maintain the baseline system and documentation as it is received from the developing agency. Interoperablity of new software modules with the existing baseline will rest with the developing agency. The Facility Coordinator will also insure that the baseline documentation is current and available at the facility.

3.2.5 Controlled Computer System Operation

Access to the computer area will be restricted to personnel working with the ADP resources. In order to efficiently utilize the ADP resources available to Facility users, the following administrative procedures will be followed.

3.2.5.1 Logs

A user log will be provided for each computer system (open system). System software will log users time on the closed system. Classified output will be logged by the computer operator.

3.2.5.2 User Identification Codes

Each facility user will be assigned a unique UIC and password by the Facility Coordinator. Passwords will be changed periodically.

3.2.5.3 Output

Printed output is obtained from appropriate system printer. Classified output must be handled in accordance with required security practices.

3.2.5.4 Expendables

The Facility Coordinator will insure that an adequate supply of expendable computer items such as paper, ribbons, etc. are available within the facility.

3.2.5.5 Facility Cleaning

All individuals are responsible for insuring their areas are kept clean and orderly. In order to maintain a high state of cleanliness there will be no smoking, drinking or eating in the computer area.

3.2.5.6 Scheduling

The Facility Coordinator will be responsible for publishing Weekly and Quarterly computer use schedules.

3.2.5.6.1 Quarterly Schedule

The Quarterly schedule will be estimated for a one year period and includes major events such as project demonstrations, experiments, and long term system development activities. Inputs to this schedule should be transmitted to RADC, who will determine requirements, hardware/software/manning/need for additional information/new or modified baseline applications programs, etc.; and performs/accomplishes contractor direction. RADC will then furnish the schedule to the on-site RADC Representative, who then makes up the weekly assignment of the TOAS assets and manpower in conjunction with the TOAS Facility Coordinator, T & D Coordinator, TAF Coordinator, and concerned contractors. RADC will coordinate and approve the weekly schedule. The TOAS Facility Coordinator then publishes and distributes the quarterly schedule. This should be accomplished no later than four weeks prior to the beginning of the affected quarter. Failure to meet this deadline may have serious impact on computer use time available to the contractor project manager. This schedule will be coordinated and approved by RADC prior to distribution.

3.2.5.6.2 Weekly Schedule

The purpose of the weekly schedule is to efficiently manage computer hardware and software assets in satisfying Quarterly schedule data and the inputs received the week prior to the affected timeblock. "Fact of life" changes will occur on a daily basis - both good and bad which will affect the schedule. All schedule conflicts will be adjudicated by the RADC Facility Manager.

3.2.5.6.3 Site Documentation

A library of documentation will be established for all users of the facility. This documentation will include reports/studies of participating contractors, facility handbooks, user software manuals, etc. It is the intent to have available on-site documentation to support the development activities. An index will be provided and suggestions for items for inclusion are solicited subject to security considerations.

3.3 TECHNICAL/FUNCTIONAL DEMONSTRATIONS

The procedures for conducting a test/demonstration for government personnel will follow the above procedures with the modifications listed in this paragraph.

3.3.1 Sponsor

Each technical/functional demonstration will have a primary contractor sponsor who will have overall responsibility for defining the demonstration. The sponsor will be required to coordinate with the T&D coordinator for contractor/government participation, test plans, scheduling system availability (and configuration), and conducting the demonstration.

3.3.2 Test Plan

The test plan must be coordinated by the players and approved by RADC.

3.3.3 Test/Demonstration Output

The test plan will specify disposition of magnetic media and hardcopy output generated during the test period. Classified materials will be controlled in accordance with local security practices.

3.4 CONFIGURATION MANAGEMENT

In order to design and develop software modules that interoperate efficiently and accurately, close coordination will be required among the contractors producing software for demonstration/test. The formal

management procedure for insuring interoperability will be the Configuration Control Board (CCB). The site CCB is a sub-board of the RADC CCB.

3.4.1 Configuration Control Board

The Configuration Control Board will consist of contractor representatives developing software for demonstration on the TOAS facility hardware and a government representative who will act as the Chairman. Others may participate at the discretion of the Chairman. Meetings will be held as required at the TOAS facility and/or in conjunction with the Project 2315 Quarterly Review meetings.

3.4.2 Terms of Reference

The objectives of the Project 2315 CCB is to insure that new software development is compatible with current baseline software for demonstration; approve new software for the baseline; and provide a forum for technical contractor coordination; and to ensure software specifications proposed for demonstration are consistent with Project objectives/milestones. The intent of the CCB is to approve changes to the baseline after successful demonstration and present acceptable alternatives to RADC.

3.5 TRAINING

Project 2315 training is the responsibility of the Test and Demonstration Coordinator and will be provided to all essential government and contractor personnel involved with the demonstration/testing of Project 2315 baseline applications package software. The specific nature of such training is discussed in the Project 2315 Training Plan. All other training is the responsibility of the individual agency or contractor.

3.6 MAINTENANCE

3.6.1 Hardware

The TOAS Facility Coordinator is responsible for preventive and corrective maintenance. A hardware maintenance log will be

maintained by the Facility Coordinator to provide a record of hardware problems. When users encounter a suspected hardware malfunction, they must document the problem in the Maintenance Log. Five hours of preventive maintenance is scheduled each week.

3.6.2 Software

The initial baseline software system provided to the TOAS facility will be maintained by the Facility Coordinator. As new software releases are provided by Digital Equipment Corporation, the baseline software modules and associated documentation will be updated. A review of the new modules by the CCB will be required prior to incorporation as the 2315 baseline software. Other baseline software modules and associated documentation will be updated/changed by the developing/sponsoring contractor upon approval of the CCB. Interoperability issues will be resolved through the CCB forum. Maintenance of the baseline facility software library does not encompass corrective maintenance of individual software modules provided by other vendors. Operating problems which indicate the need for software repair or modification will be documented as specified in the Configuration Control Plan and forwarded to the appropriate module developer for appropriate action.

APPENDIX 3-A: PROJECT 2315 DEFINITIONS

3-A.1 BASELINE SYSTEM

Defines the software and hardware that RADC designates as required to support the development, evaluation, and demonstration of Tactical Air Force functions, e.g., collection management, targeting, etc., and/or communications and external/internal displays. Once established, the hardware and software components of the baseline system will be controlled by RADC through the use of the configuration control function.

3-A.2 CONFIGURATION CONTROL BOARD

The CCB is composed of Project 2315 contractor and government representatives. The purpose of this board is to control the hardware and software configuration available for RADC approved tests and demonstrations. This board will operate as a subcommittee of the Project 2315 Contractor Coordination Group.

3-A.3 RADC FACILITY MANAGER

RADC (or its designated representative) is the Facility Manager and has the overall and final authority over Project 2315 matters. The Facility Manager is responsible for providing equipment, property, and services required by on-site contractors; ensuring appropriate long range coordination is effected between contractors; providing required funding for facility equipment, operations, and services. The facility manager coordinates and approves long-term facility scheduling requirements and adjudicates scheduling problems.

3-A.4 TOAS FACILITY COORDINATOR

TRW has been designated as the Facility Coordinator. The Facility Coordinator prepares and maintains the facility operating schedule. Coordinates on test and demonstration plans to insure the required baseline hardware and software is available and appropriately configured. Provides computer operations and maintenance activities as outlined in

paragraph 3.2. Establishes and manages the facility baseline configuration in accordance with the Configuration Management Plan (Appendix 3-B). Provides copies of the baseline software to other agencies when approved by RADC.

3-A.5 ON-SITE RADC REPRESENTATIVE

A permanent Air Force Systems Command employee authorized by RADC to represent them in Project 2315 matters, at Langley AFB. This person is responsible for coordinating the facility utilization schedule (including test and demonstration), functioning as the liaison between contractor and Langley Air Force Base personnel,and monitoring contractor on-site performance. Further responsibilities of this representative are contained in the latest TAC Headquarters and RADC memorandum of agreement.

3-A.6 TACTICAL AIR FORCES COORDINATOR

TAC/INY is responsible for coordinating tactical Air Force (TAF) user (TAC/PACAF/USAFE) inputs and participation for Project 2315 demonstrations/experiments.

3-A.7 RESIDENT CONTRACTOR PERSONNEL

Those personnel permanently assigned to the TOAS facility. TRW and Bunker Ramo provide resident contractor personnel.

3-A.8 TEST AND DEMONSTRATION COORDINATOR

The Bunker Ramo representative has been designated by RADC as the Test and Demonstration (T&D) Coordinator for Project 2315 applications software.

3-A.9 TDY CONTRACTOR PERSONNEL

Those persons working on Project 2315 contracts requiring periodic use of the TOAS Facility and its computer resources.

4. NEW TECHNOLOGY FOR THE TOAS FACILITY

This section provides the reader with some background and technical explanation of the technology driving the TOAS system environment. Of particular note are the fiber optics links (implemented in the VT-100-T, Tempest terminals) and the Winchester disks (implemented in the System Industries 675 MB disk system).

4.1 FIBER OPTICS THEORY AND APPLICATIONS

The advent of commercially available fiber optics communication links and components has increased the number of solutions to difficult communications problems. Practical application is now possible since development of better fiber optics system components. Many communications problems are now solvable with off-the-shelf components. This section reviews existing theory, present day applications, and future development trends.

4.1.1 Fiber Optics Communication Systems

The attractive features of fiber optic communication systems have been known for some time: little susceptability to electrical interference, heat, and caustic environments; no electrical shock, fire, or explosion danger resulting from cable breaks; an absence of electrical emanations; and greater bandwidth than conventional communication systems.

As in most communication systems, fiber optic communication systems consist of a transmitter, transmission medium, and a receiver. The transmitter imposes some form of modulation (signal) on the light source for transmission of information by either switching the light source on and off, (digital communications), or by varying the light source intensity (analog communications). This transmitted information in the form of modulated light reaches the receiver via a fiber optic cable. Typical fiber optic cable is composed of plastic or glass fiber strands. The receiver contains a light sensor that receives the modulated light signal from the fiber optic cable and transforms the light signal back into the electrical signals that originally represented the transmitted information.

4.1.2 Light Transmitters

The light transmitter consists of two main components, a light source and a light source modulator. Light emitting diodes (LEDs) and laser diodes are the best suited and most widely used light sources. The modulator consists of the electronics that transform electrical signals into modulated light signals. This is accomplished by either intensity modulating the source (amplitude modulation - AM) or by switching the source between on and off states (pulse code modulation - PCM).

4.1.2.1 LED and Laser Light Sources

Basic construction of LED and laser sources is based on the semiconductor junction diode. A forward bias applied to the LED's p-n junction increases the energy level of the n-material electrons, causing them to flow into the p-material. The higher energy electrons give up their extra energy in the form of light emission upon reaching the p-material. The LED output is almost linearly proportional to the input current, allowing the LED output to be intensity modulated for use in analog signal transmissions.

The laser light source is a modified p-n junction known as a semiconductor injection laser. When the laser is forward biased, and after the input current reaches a certain threshold, coherent light emerges from the p-n junction. Lasers are less suited for intensity modulation because of the turn-on threshold they exhibit. But the light power output from the laser is greater than the LED making the laser idealy suited for high-speed digital communications by PCM.

4.1.2.2 Characteristics of LED and Laser Light

Light output from the two sources differ greatly in several ways making choice of light source application dependent. Light emission from a LED is lambertian; which implies that the light rays are emitted at all angles over the entire output hemisphere, where as laser light is coherent (very narrow wavelength bandwidth) and highly directional. Because LED light is emitted over a broad area, source to fiber coupling is relatively easy but not as efficient as the more difficult laser coupling.

A smaller percentage of the total LED light output is incident on the input end of the fiber than for incident laser light. Good coupling efficiency of laser light is due to the highly directional nature of the output beam allowing more incident light on the input to the fiber, but again the coupling alignment between source and fiber is more difficult to achieve.

Emitted light from a LED is considered to have a broader spectrum when compared to the narrow spectrum of light emitted from a laser. That is, the LED half intensity wavelength bandwidth can be 10 to 15 times greater than that of laser light. Spectrums of typical industrial emitters are graphed in Figure 4-1 below. The half intensity spectral width for the LED is about 50 nm and about 4 nm for the laser.

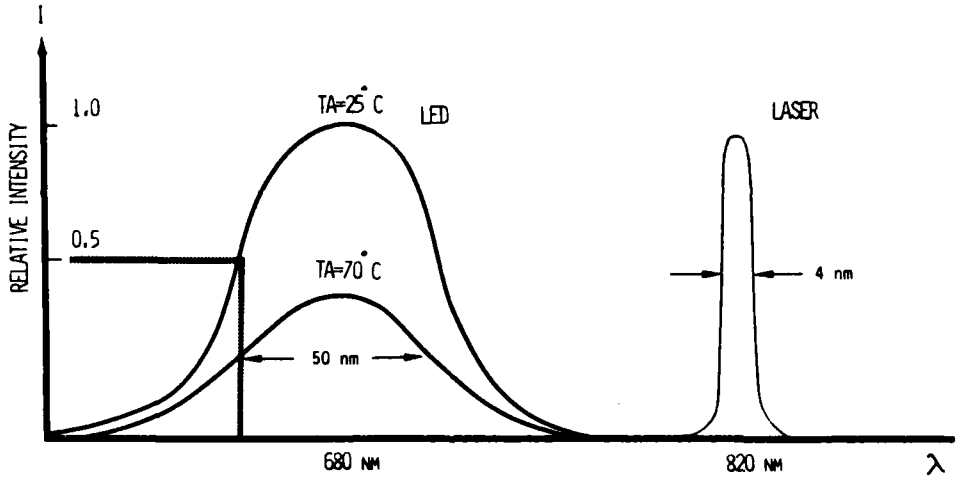


Figure 4-1. Output spectrums of typical LED and laser sources.

4.1.2.3 Light Source Switching Speeds and Bandwidth

Maximum switching speeds for the two light sources differ greatly. LEDs are slower than lasers with the maximum LED switching speed about 100 megabits/second (Mb/s) while lasers are being switched at gigabit/second (Gb/s) rates. This great difference is attributed to the lasers greater ability to convert electrons into photons. LED maximum switching rates are about 100 Mb/s for digital systems and 25 to 40 MHz for analog systems.

Different wavelengths of light travel at dissimilar speeds through a given medium with the longer wavelengths propagating faster. This phenomenon results in a distortion referred to as material dispersion. Since a LED emits many more wavelengths than a laser (50 nm bandwith in Figure 4-1), a time dispersion of the emitted LED waveform results, because the longer wavelengths reach the receiver before the shorter wavelengths. This effect is much less noticable for lasers because there is essentially one wavelength of light emitted (4 nm bandwidth) and therefore material dispersion is much less noticeable. The resultant LED time dispersed wave form has a smaller amplitude and longer time base or period than the input waveform. If a LED's spectral width is excessive, it could be switched at a rapid enough rate to cause excessive time dispersion and eventually pulse overlap. Switching speeds are therefore much higher for the near-monochromatic laser light source.

4.1.2.4 Flux Pattern

An important characteristic of both light sources is the emitted near-field radiation or flux pattern. The flux pattern of typical LED and laser sources are shown in Figure 4-2. The graph relates the amount of

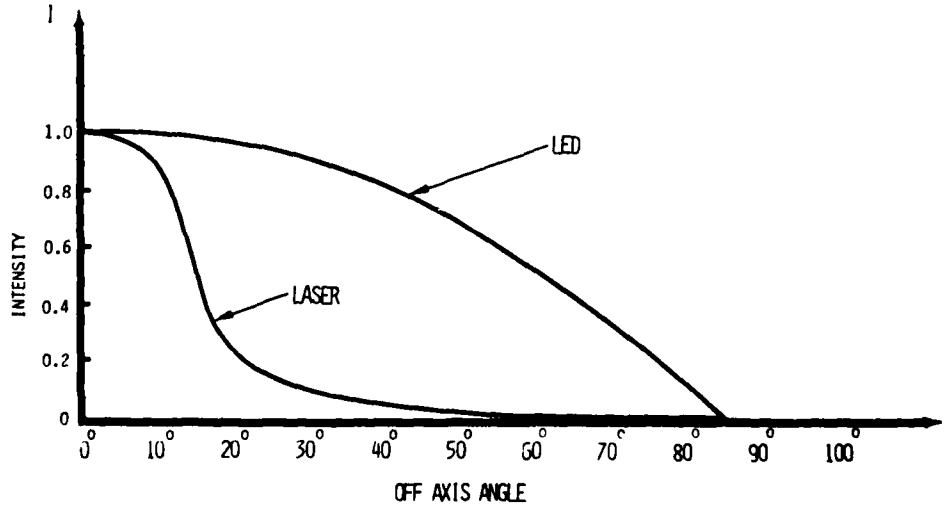


Figure 4-2. Far field radiation pattern of typical LED and laser sources.

output light power available to the angle off the center output axis, with the light power at a maximum in the center and decreasing with the cosine of the off-axis angle. It can be seen from the graphs that the laser produces a narrower beam pattern or less off-angle flux (i.e. the light output power is concentrated near the center or is more axial).

A well designed laser source will have a narrow output beam to minimize stray flux yet have a broad enough beam to facilitate easy coupling to the fiber. Although lasers are more difficult to couple with an optic fiber, they have a higher power output and higher coupling coefficient which translates to lower coupling loss or a higher ratio of accepted input flux to fiber.

4.1.3 Light Detectors/Receivers

At the receiving end of an optical communications system, the incoming optical signals are translated back into the electrical representation of the input signal. Accurate translation between optical and electrical signals is accomplished by the receiver, which contains electronics that amplify and compensate the light detector output current. The most common detector in use today is the photo diode detector with the two most widely used photo diodes being the PIN and APD photo diodes.

4.1.3.1 PIN Photo Diodes

A PIN diode consists of a p-n junction with an intrinsic layer between the p and n layers (PIN). When light strikes the p-n junction of a properly biased PIN diode, photons are converted into electrons and a current flow results through the p-n junction that is proportional (and essentially linear) to the incident junction photon flux (i.e. increased amount of incident light, increased amount of junction current).

Available PIN diodes exhibit spectral response and sensitivity similar to that shown in Figure 4-3. The frequency response of PIN diodes extends from DC (0 mHz) to 1 GHz, so that laser pulses of 0.1 nS duration are observable.

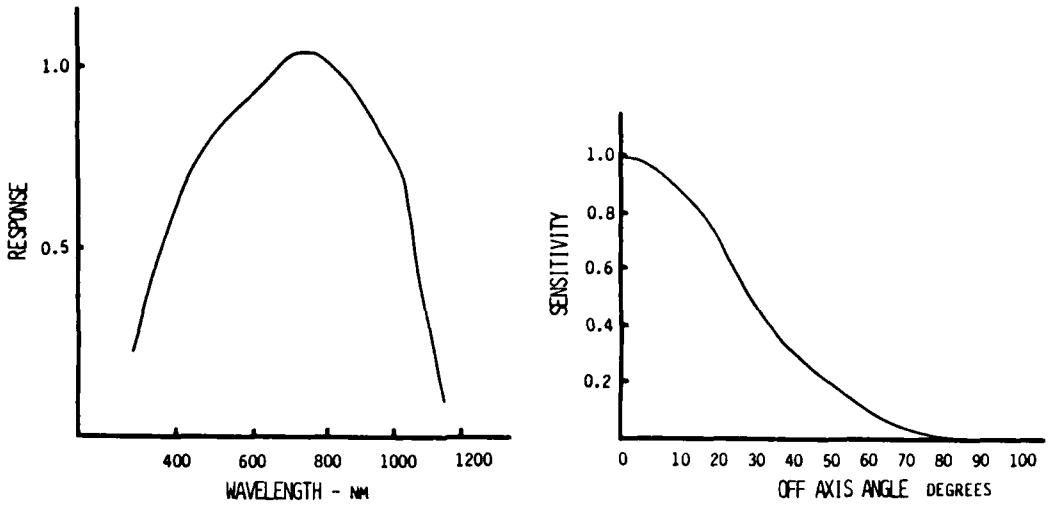


Figure 4-3. Spectral response (L) and directional sensitivity of a typical PIN diode detector.

4.1.3.2 APD Photo Diodes

The avalanche photo diode (APD) is more efficient than the PIN due to APD gain characteristics. For a given unit of incident photon flux, the current through the APD junction will be higher than that of the PIN diode, therefore the APD exhibits gain in the input signal power similar to the amplifying action of a transistor. For photo detectors, the sensitivity is defined as the minimum photon flux input to provide a given output. Then, because APDs have gain characteristics, they are more sensitive than PIN photo diodes.

4.1.4 Fiber Optic Transmission Path

Fiber optic cable provides the transmission path over which light signals propagate. Several important characteristics such as construction size, index of refraction, numerical aperture, attenuation, and modes of propagation must be considered before the proper cable can be chosen for a specific application.

4.1.4.1 Fiber Optic Construction

Construction of a simplex and duplex fiber optic cable is illustrated in Figure 4-4. Typical cable construction begins with the optical fiber core, which is either glass or plastic, that is surrounded by a cladding

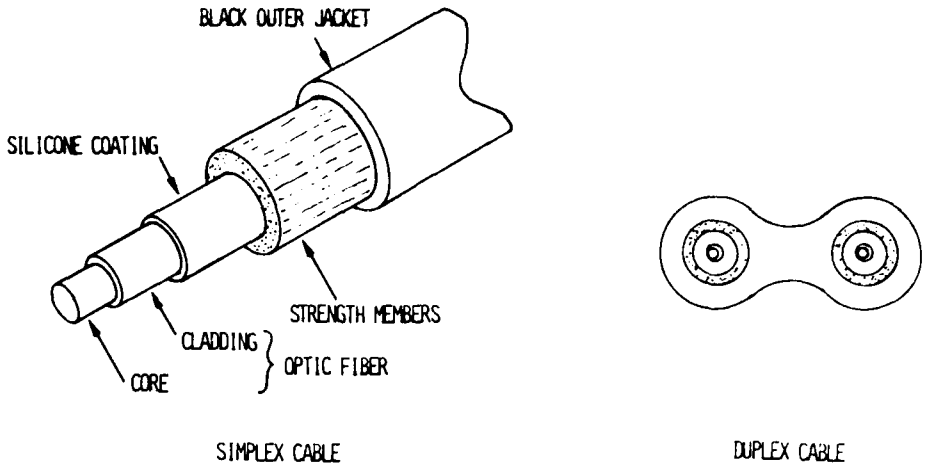


Figure 4-4. Fiber optic cable construction, simplex or single fiber (1), and duplex.

material that may also be composed of silica glass or plastic. Typical cable is usually silica core with a plastic cladding. Specific properties of the cladding material determine an important characteristic of the cable known as numerical aperture which is discussed in subsequent sections. Other layers are added to the core/cladding for strength and protection including an opaque outer sheath. New types of fiber optic cable are extremely durable in the mechanical sense and are of very light weight.

4.1.4.2 Fiber Optics: Size - Index of Refraction - Propagation Losses

Optical fiber core diameters range from 50 micrometers to 1000 micrometers (0.05 mm to 1.0 mm) with 200 micrometers being a typical size. Core and cladding material characteristics combine to yield a fiber optic cable with specific characteristics. An important characteristic of the core material (transmission medium) is its index of refraction (n). This n figure relates at what velocity a particular wavelength of light will propagate through the core. Light travels slower by some percentage through any transmission medium denser than a vacuum, and n is a ratio whose numerator is the speed of light in a vacuum (300,000,000 m/s)of the speed of light to the wave length speed and denominator is the wavelength speed in the particular core medium. As an example n = 1.0003 for air which states

that the speed of a particular wavelength of light is just slightly slower in air than in a vacuum. For typical glass, n = 1.58 which states that a certain wavelength of light propagates through the glass at 58% of the speed of light. Another important property of n is that different wave lengths of light 'see' or encounter different n values in the same transmission medium. Longer wave lengths (infared) encounter n values closer to n = 1 than do shorter wavelengths (ultraviolet) and therefore the longer wavelengths propagate faster through the transmission medium than the shorter wavelengths.

Light propagation through the core may be understood by first examining the reflection that light rays under-go as they encounter the core/cladding boundary. This action is illustrated in Figure 4-5 by rays a and b and is explained as follows: when a light ray passes from one

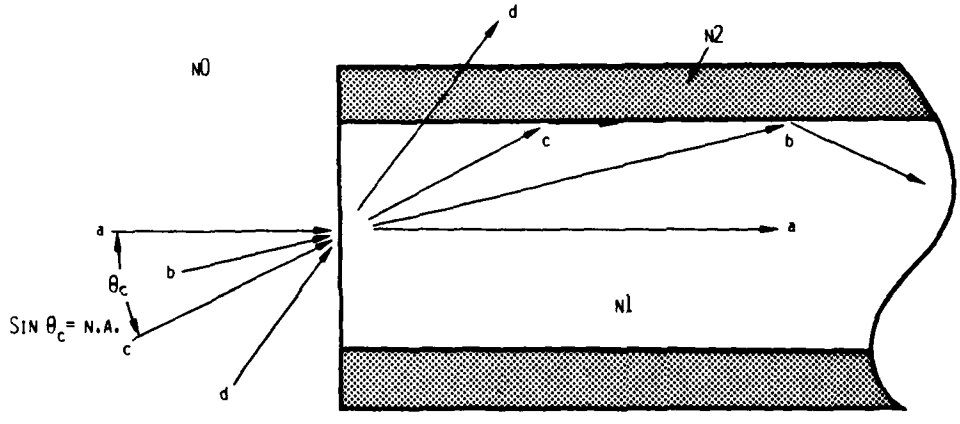


Figure 4-5. Fiber core and cladding longitudinal cross section depecting numerical aperture (NA) and internal light ray reflection.

medium (n1) to another medium (n2), where n2 is less than n1, the ray will be reflected back into the first medium n1 which is the fiber core. This reflective action continues until the ray exits the core at the other end.

4.1.4.3 Attenuation

As light traverses the fiber core, several losses occur which attenuate the output light power. Each time a propagating light ray reflects off of the cladding, the intensity of the ray is decreased by a minute amount. Material impurities also attenuate the intensity of the ray. The above two losses are the largest factors in fiber optic cable losses per unit length.

4.1.4.4 Numerical Aperture

Input light acceptance by the optical fiber core is another important characteristic known as numerical aperture. Incident light rays are transmitted into the core and exit the core only within a certain angle. This is illustrated in Figure 4-5. Ray a is incident on the center line and passes directly through the fiber core. Ray b falls within the acceptance angle and is reflected down the fiber core. Ray c defines the acceptance angle and does not reflect back into the core but does not pass through the cladding. Ray d however falls outside of the acceptance angle and is not reflected back into the core but passes through the cladding to be absorbed in the opaque outer sheath. Therefore the light acceptance capability or gathering capacity is expressed as a number called numerical aperture (NA). Numerical aperture is defined as either the sine of the maximum light acceptance angle for a particular cable or the sine of the maximum angle at which light will exit a particular cable. Typical values for NA are 0.2 to 0.5 (12 to 30 degrees).

For the acceptance angle to exist (NA greater than 0), n1 must be greater than n2. Rays may propagate at various angles within the limits imposed by NA. Those rays propagating at small angles with respect to the core axis are called low order modes, while rays entering near the acceptance angle limit are called high order modes. When mixed modes of propagation occur, a distortion known as modal time dispersion results. This is due to the fact that the light rays traveling at small angles to the center line travel less distance in the fiber core than the rays of the higher orders (larger angle from the center line). Since rays of the higher

orders take longer to propagate through the fiber core because of the extended path length that must be traversed, a distortion that is referred to as modal time dispersion exists which results in time base or period stretching of a pulse input.

NA is also directly related to the cable bandwidth. By decreasing the cable's NA, only the lower order modes of propagation result, allowing for increased cable bandwidth.

4.1.4.5 Fiber Optics Cable Classifications

Fiber optic cable is divided into three major groups, single-mode step-index, multi-mode step-index, and graded-index according to the fiber core and cladding index of refraction. These groupings are necessary so as to deal with the modal dispersion effect in several ways.

An abrupt change of reflective index between core and cladding is called step-index cable. When the core diameter equals the wavelength of propagated light, only a single mode will propagate thus eliminating modal dispersion. This cable type is single mode step-index cable and has one main disadvantage: emitter/core coupling is a laboratory task and is difficult. An increased core diameter allows for easier emitter/core coupling but allows higher order modes to propagate thus increasing modal dispersion. A compromise between single-mode step-index and multi-mode step-index is graded-index multi-mode cable. Graded-index type cable has an index of refraction that is maximum in the center and decreases with the radial distance from the center. Since light waves travel slower through a higher n, the shortest path rays in the center travel slower while the longest path rays reflecting near the acceptance angle travel faster through the lower n near the cladding allowing for uniform propagation of all rays through the fiber (i.e. time dispersion is decreased).

4.1.4.6 Complete Fiber Optic Link

The complete fiber optic link then consists of an emitter, either LED or laser, a transmission path, usually graded-index multi-mode cable, and a detector that is either a PIN or an APD photo diode. The losses in a fiber optic link are input/output losses due to emitter/fiber and fiber/detector

coupling, transmission losses proportional to the length, and cable to cable splice losses.

Detection of faults in a fiber optic link is possible with instruments that utilize the pulse reflection principle. When a cable breaks, there is an abrupt decrease in n at the break point allowing an input pulse to be reflected back from the fault and timed. The time to send and receive the pulse is measured and read directly out in distance accurate to 1 percent.

4.1.5 Communication Link Modulation Methods

The type of modulation method required for an input signal depends upon the type of input signal (analog or digital) and also upon the frequency range of interest. Several general methods are available and are briefly explained below.

4.1.5.1 Frequency Division Multiplexing (FDM)

FDM combines analog signal channels and transmits them at the same time in different frequency ranges. This is a common way of implementing the transmission of analog signals. For this type of modulation, usually a LED is intensity modulated corresponding to the frequency and intensity of the analog input signal.

4.1.5.2 Time Division Multiplexing (TDM)

TDM combines information channels containing constant amplitude signals that are represented by the presence and absence of digital signal voltage levels. The time position of a pulse, relative to other pulses, determines the signal voltage level presented to the channel. TDM is commonly used in digital applications because it is easier to switch detect on/off states than variations in light intensity as is the case in FDM.

4.1.5.3 Pulse Code Modulation (PCM)

PCM is the on/off switching of the emitter with each on/off state occurring for a certain time duration or at a fixed transmission frequency. This method lends itself most directly to many applications in digital communications and digital computer communications. As in TDM, it is easier to detect the on/off states of the emitter than it is to detect intensity variations.

4.1.5.4 Wave Division Multiplexing (WDM)

WDM allows two or more optical signals to be transmitted simultaneously over a single fiber. Emitter outputs of different peak wave lengths are mixed into a single fiber for transmission and separated by detectors that are sensitive to the respective wavelengths.

4.1.6 Fiber Optic Cable / Wire Comparison

Fiber optic cable usually possesses a definite advantage over wire cable in the areas of attenuation, bandwidth, electromagnetic interference, size, and durability.

4.1.6.1 Attenuation and Bandwidth

Quality fiber optics cable has substantially less attenuation per unit length than twisted wire pairs. This characteristic is important when deciding how many repeater stations are needed in a communications link. But optical repeaters are more complex and expensive than a wire system repeater so a careful analysis of the two links must be made.

Optic fiber has a greater bandwidth than twisted wire pairs, but less than coaxial cable. Wide bandwidth allows a greater volume and variety of signal transmission over a given system. The bandwidth of fiber optics cable in actuality is greater than that of coaxial cable, but limitations arise mainly in the amount of transmittable power (light flux). While the input power to wire cable systems is easily produced at almost any level, input power to fiber optics cable is usually less than a few milliwatts. Low power input (small input signal amplitude) plus transmission path attenuation degrades or limits the signal to noise ratio and therefore the attainable bandwidth.

The cutoff frequency limit (bandwidth) of fiber optics cable is inversely proportional to the length of the cable while twisted wire pairs and coaxial cable are inversely proportional to the square of the cable length. It is interesting to note that since fiber optics cable is incapable of picking up noise (unlike wire), the receiving end signal to noise ratio is solely determined by noise produced in the receiver.

4.1.6.2 Electromagnetic Interference and Emanations

When passing a signal, fiber optic cable neither emits or picks up electromagnetic signals which is untrue for wire cable. Light signals passing through a fiber optic cable are electrically neutral photons, therefore, interference from strong electric fields (high voltage, lightning, static discharge) and strong magnetic fields (electrical machinery, transformers) is impossible. This is not true for wire where currents and voltages may be induced into a transmission path. Currents cannot be induced into plastic or glass fibers because the material is an insulator.

The neutral electrical properties of light signals infer that electric or magnetic fields do not exist around a fiber optic cable unlike the fields surrounding a transmission line. Therefore data transmissions over fiber optic cable is secure from electromagnetic tapping or inductive coupling and offers a degree of data transmission security.

Data transmitted over wire is present in the electric and magnetic fields surrounding the wire so physical contact with the wire is not necessary to obtain signal information. However, contact with a fiber optic cable is necessary to obtain signal information. A portion of the opaque sheath must be removed or dissolved allowing photo diode or photo-multiplier coupling to the cable. This procedure would be rather difficult but not impossible. Removal of the opaque sheath would introduce noise and attenuation into the system at that point and allow detection of possible tampering with the fiber optic link.

4.1.6.3 Size and Durability

Due to the higher transmission speeds inherent in fiber optic links, a multi-pair fiber optic cable is smaller in diameter than a multi-pair copper cable. Fiber optic cable is easier to install because of its very light weight. Jacketed fiber optics cable now has the ability to withstand greater physical abuse both mechanically and chemically.

4.1.7 Applications

Fiber optics can provide the solutions to many data communications problems dependent upon requirements such as speed or bandwidth, security, and physical environment. Data communication signals listed in order of increasing bandwith requirements are:

- Voice
- Data; low, medium, and high speed
- Video

Various properties of fiber optics data transmission systems are well suited to digital computer data communication systems. Fiber optics offer high speed data transmission capabilities, and a reliable, secure transmission link.

Intersystem links find many applications in the area of terminal and peripheral equipment communications. Short links (100 meters or less) may interconnect a computer to remote user terminals and peripherals that easily satisfy the bit rate or bandwidth requirements. For example, Hewlett Packard offers an evaluation kit containing an emitter, detector, and five meters of 1.0 mm core plastic fiber optics with much of the required support electronics included in the tranmitter and receiver. This five meter length has a bandwidth of 10 MHz (DC to 10 MHz) which translates to 1 million 10-bit characters per second for serial communications, which is more than enough bandwidth or speed for terminal communications and most peripherals.

The maximum speed of the EIA RS232 to fiber optic interface of the VT100 Tempest terminal and the DZ11 Tempest multiplexer link is 960 10-bit characters. The fiber optic components in this link will perform at this rate at lengths up to 1000 ft. Higher speed operation would be possible in shorter lengths. The multiplexer and terminal communicate in the same manner that modems communicate utilizing the frequency shift keying (FSK) method. A mark (EIA line voltage below ground) is transmitted at 307.2 kHz and a space (EIA line voltage above ground) is transmitted at 153.6 kHz. The fiber optics interface specifications are listed on the next page.

- Transmitter:

LED light frequency:	670 nm (red) or 820 nm (infrared) depending on supplier
Output power:	20 microwatts
Mark frequency:	307.2 kHz
Space frequency:	153.6 kHz

- Receiver:

Sensitivity:	20 nW average input
Maximum input power:	100 microwatts
No signal:	10nW or less output as mark (line idle)
Accepted light frequencies:	670 nm or 820 nm

- Fiber optics cable:

Length:	50 ft
Material:	Plastic clad silica
Maximum Length:	1000 ft at 9600 bps

Complete asynchronous fiber optic links implementing the EIA RS232 protocol are available and mate directly to RS232 computer interfaces and terminals. The wire communications path is replaced by a fiber optic path and data transmission rates up to 56k-bits/s are possible.

Fiber optics also finds direct application in computer to computer links. The PDP11 to PDP11 communication link, Decnet (DMC11), could be implemented in full duplex with a single duplex fiber optics cable about the size of an ordinary lamp cord instead of the two coaxial cables or single triaxial cable required. This type of fiber optic link would virtually eliminate computer to computer data transmission security problems and still allow transfer rates at maximum throughput.

4.1.8 Future Development Trends

How competitive and successful fiber communications will be in the future appears to depend upon the development of components in the 1300 nm wavelength region of the spectrum (well into the infrared). This region is of interest because cable attenuation is greatly reduced at the longer wavelengths where material dispersion drops near zero. Research has shown single mode cable (core diameter equal to the input light wavelength) exhibits three attenuation minimums occur at 1100 to 1200 nm, 1300 nm,

and 1500 to 1700 nm as shown in Figure 4-6. Most research is in the 1300 nm region because of manufacturing difficulties involved in long wavelength fiber optic devices.

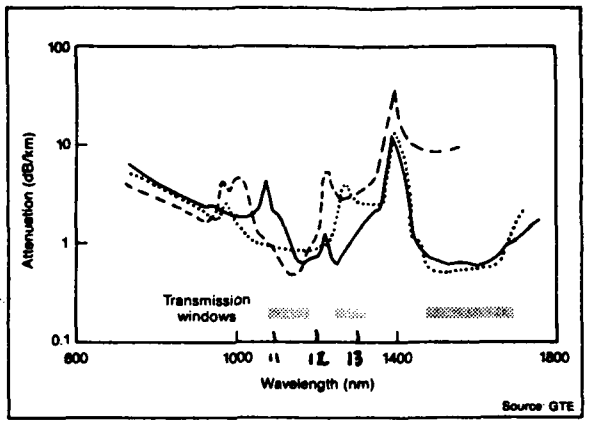


Figure 4-6. Plot of single mode fiber optic cable showing three attenuation minimums.

As seen in the above figure, cable attenuation at the 800 to 900 nm region is about 6 dB/km and only about 1dB/km in the 1300nm region. A 6 dB attenuation equates to 25 milliwatts of output power for 100 milliwatts of input power and a 1 dB attenuation is 79 milliwatts of output power for 100 milliwatts of input power. The decrease in attenuation allows for longer transmission paths and an improved signal to noise ratio.

4.1.8.1 Component Improvements

Longer wavelength LED and laser components must rely on combinations of fabrication materials and complex manufacturing processes to achieve the desired spectral region. Laser sources are undergoing improvements to overcome characteristics power-output dips, difficulty in handling, high-temperature operation, and short operating life. Areas of LED improvement include better switching bandwidth, smaller spectral bandwidth, and improved fiber coupling efficiency. New designs to improve detector sensitivity by increasing performance of the FET amplifiers usually integrated into the

detector, and light gathering techniques. In conventional detectors light rays are collaminated by a lens onto the active region. Designs are now attempting to reduce noise at the input by covering the active region of the detector with materials that are transparent only to wave lengths greater than 960 nm. At 1300 nm PIN diodes appear to hold the edge over ADP diodes because of easier construction.

4.2 SERIES 9775 WINCHESTER (SYSTEM INDUSTRIES)

The System Industries Series 9775 Winchester is a fixed media disk drive offering a storage capacity of 675 Mbytes. The 9975 in conjunction with the System Industries 9400 Disc Controller interfaces to the PDP 11/70 Mass Bus in an RH70 Controller slot and provides total RH70 emulation which is operating system software transparent.

4.2.1 Disk System Hardware Description

The Series 9775 675MB disk drive comprises a cabinet and frame (36.0 x 23.0 x 38.0 inches) containing a sealed Head Disk Assembly (HDA), the drive motor and brake, a power supply, and an air circulating system. A logic chassis contains the electronics for read/write, I/O, fault, drive and control functions, plus a microprocessor controlled servo.

Components sealed within the HDA are a deck plate, spindle, disks, heads, and the linear motor voice coil. There are 40 heads of low mass that are lightly loaded to allow start/stop contact with the recording medium and low flying heights. Two heads per recording surface read/write 20 data surfaces at 6495 bpi (inner track). Recording medium is a coated, oriented magnetic oxide disk, which facilitates start/stop contact of the read/write data heads.

Included on the drive is a stand alone diagnostic panel that allows for execution of disk drive diagnostics from the control panel. Diagnostic tests are entered and initiated via the diagnostic panel by rotary dial selection of the desired test number. The panel will constantly display the current state of the drive, monitor all system voltage supplies, and display a hexadecimal error code for any hardware discrepancies found.

4.2.2 Series 9775 Hardware Features

Several hardware features included in the 9775 system incorporate recent technological developments and improvements in the disk drive field. Major operating features include:

- 6,000 hours MTBF utilizing Winchester technology.
- Co-resident operation with System Industries 300 MB removable media drives.
- Drive group configurations allow up to eight daisy chained drives up to four drives in a radial fashion.
- Drive groups may interface with up to four CPUs.
- Access times: 10 mS track-to-track; 25 mS average; 50 mS maximum seek.
- No preventive maintenance required.
- Dual port logic which enables two controllers to access the same drive.
- Sealed HDA, which can be exchanged in 15 minutes, for improved reliability.
- Features phase-locked oscillator/data encoder with write precompensation.
- May be configured as two 300 Mbyte logical drive units.

4.2.3 Hardware Installation

Integration of the SI9775 Winchester disk drive into the TOAS computer system was very straight forward proceeded without difficulty. The total time required to complete installation and verification was approximately six hours. Briefly, installation proceeded as follows: Rack mount the 9400 controller in lower cabinet of TU10 tape drive; configure and install the fast bus interface (RH70 emulator); cable fast bus interface and drive to controller; verify proper hardware operation with SI supplied diagnostics.

The 9400 primary UNIBUS address and interrupt vector is the same as that of the RP06 disk drive (176700 - 254). A secondary address and interrupt vector was chosen so that the RP06 would remain undisturbed.

This secondary address and interrupt vector was strapped on the fast bus interface before installation. SI supplied a bootable diagnostic magtape and diagnostic users manual to successfully accomplish the system acceptance tests and to help diagnose future hardware problems.

4.2.4 System Software Modifications

Although the SI 9775 disk system emulates DEC equipment, some software changes are required to system handler, utilities, and system generation files. The TOAS Facility installed the SI 9775 disk system with DEC's IAS V3.0. This subsection details the required software changes and system generation procedures used to integrated the disk system in the TOAS Facility.

4.2.4.1 Software Modifications

It was necessary to modify some of the DEC software in order to use the System Industries 9775 Disk Drive. This drive, due to its increased size, has a greater number of heads and a greater number of sectors per cylinder than the DEC RM03 disk drive which it emulates. Due to these altered device characteristics, the disk drive handler and any system utility which reference the drive must be altered. The task images which must be altered are:

- DR.TSK
- DSC.TSK
- BAD.TSK
- INI.TSK
- SGN1.TSK
- RM03BOOT.TSK.

The system files which must be altered are:

- BADSYS.SYS
- DSCSYS.SYS.

ZAP, a DEC utility, is used to make the necessary modifications. ZAP allows the user to change the contents of logical memory addresses inside system files and task images. An example of its use follows.

```
MCR  ZAP(CR)              ;initiate ZAP
ZAP   11,1 DR.TSK/AB      ;specify file name
-3626/(CR)                ;specify address
000:003626/000005         ;ZAP displays contents
-23(CR)                   ;load new contents
-X(CR)                    ;exit ZAP
```

The complete list of the necessary software modifications are found in Appendix C of this report.

4.2.4.2 IAS System Generation

Building a mountable/bootable IAS operating system first required modification of the current operating system on the RP06 drive to recognize the new 9975 disk drive. Once this new device was generated into the system, the device can be mounted and accessed like any other random access device; a bootable DR system had to be built. The following system files were modified to generate a DR bootable system:

- 11,17 SYSBLD.CMD

  - INS 11,17 DR ; the RP06 disk handler no longer the system device.
  - INS 11,17 BIGFCP/TASK=DB0ACP
  - INS 11,17 BIGFCP/TASK=DB1ACP
  - INS 11,17 BIGFCP/TASK=DR1ACP ; installing multiple copies of the file handling system increases throughput.
  - LOA DB
  - LOA DR ; Load the device handlers.

- 11,17 SYSGEN.CMD

  - TARGET=DB1: 11,1 IAS.SAV is changed to
    TARGET=DR0: 11,1 IAS.SAV
  - DEV=DB1, RP06 and DEV=DB0, RP06 is changed to
    DEV=DB0,RP06,254,5,176700,DB0ACP
    DEV=DB1,RP06,254,5,176700,DB1ACP
    DEV=DR0,RM03,150,5,176300
    DEV=DR1,RM03,150,5,176300,DR1ACP ; the device statements are changed to reflect the non standard RM03 vector and address. Each device is associated with a separate ACP to increase throughput (DR0 defaults to BIGACP)

  - SY=DB1: is changed to SY=DR0: ; this statement redefines the DR0: as the default system device.

- INS=GEN, 11,17 DB is changed to INS=GEN, 11,17 DR ; this statement installs the DR device handler in the General memory partition as required by SYS GEN Phase 2.

After the file modifications were made, a target System Generation was performed with the system on DB1 and the target device on DR0. After completion of the SYSGEN, a software boot (mount DR0: and BOO DR0: 11,17) was successfully accomplished. Subsequent to the software boot, a hardware boot can be accomplished by using the following routine:

- Depress the Halt Switch
- Depress the Continue Switch ; this action clears the system registers including the drive status registers and sets up unit 0 (DR0:) to read from Word 0, track 0, and Sector 0.
- Optional: Load Address 176310 and Deposit 1 (if unit to be booted from is DR1:) in the Drive Control Status Register, RMCS2
- Load 176300 and Deposit 23 (pack acknowledge) ; this action sets a volume valid bit in the Drive Status Register, RMDS.
- Deposit 71 ; a read command.
- Load Address 0 and hit start.

This routine accomplishes a 64K Work DMA transfer starting at logical disk block 0 (containing the Boot Block) and starts execution. This procedure is simple to use and avoids the difficult task of boot rom modification.

4.3 32-BIT MICRO/MINI COMPUTERS

Technological advances in the fields of Large Scale Integration (LSI) and Very Large Scale Integration (VLSI) have made it possible to increase the capabilities of microprocessors and microcomputers currently available. With increased demands for computing power within acceptable price ranges, an effective alternative to mainframes was required. Microprocessor architecture has undergone an evolutionary phase from 8-bit processors to 16-bit processors to the 32-bit processors now available.

There are two methods currently in use for implementing 32-bit processors. The first method is to use a true 32-bit processor with 32-bit address and 32-bit data buses; while the second method is to use a 32-bit address bus

and a 16-bit data bus. Such a processor is commonly referred to as a pseudo 32-bit processor. One of the major advantages of using a 32-bit address word is the ability to support a large logical address space, up to four giga-bytes (4G bytes). This provides for greatly increased computing power; however, if the system uses a pseudo 32-bit microprocessor, the 16-bit data bus will degrade system throughput.

There are several manufacturers of 32-bit processors. Some of them have developed very elaborate methods to implement these processors. For example, Data General, in their Eclipse MV8000, uses an instruction processor as well as an execution processor. The instruction processor decodes instructions for subsequent execution. The processor contains a 1K byte, direct-mapped instruction cache organized as a 64 block, high-speed memory with 16 bytes per block. Because of look ahead and look behind potential, the instruction cache speeds up program execution, particularly benefiting program loops and backward branches.

Another innovative processor is the iAPX 432 by Intel. This is a 32-bit processor with a 16-bit data bus. The processor is actually a dual chip set. The iAPX 43201 serves as an instruction decoder and a microinstruction sequencer. The iAPX 43202 serves as the actual execution unit. The iAPX-432 has a high level instruction set which is almost a one-to-one correspondence with high level languages such as Ada. One of the most unique features of this microprocessor is that to achieve efficient storage, instructions are encoded without regard for byte, word, or other artificial boundaries. Each instruction occupies exactly the number of bits required for its complete specification.

There is a variety of 32-bit micro/mini computers available in a wide range of entry level prices and a wide range of capabilities. Systems are available that will support a varying number of terminals, with a varying memory size, with entry level prices from $20,000 to $200,000 plus.

4.4 Intelligent Database Machine (IDM-500)

Currently the trend in data processing is to segment specialized ADP functions into hardware/firmware "machines". Smart terminals, I/O controllers, and unique peripheral processors are examples of this process. Britton Lee Inc. has implemented a relational data base management type of system in their IDM series (200 & 500) processors. These devices off-load data base I/O processing to maximize total system performance. The TOAS Facility can provide the necessary functional and ADP environment to test and experiment with the IDM-500. These experiments will allow system designers to check the appropriateness (inappropriateness) of this type of technology in support of Tactical Intelligence data processing requirements.

4.4.1 IDM 500 Hardware Description

The basic IDM is a rack mounted device (17.5" high, 19" wide, and 24.75" deep, weight 170 lbs) with the following capabilities:

- Data Base Processor
- Storage Module Device (SMD) Disk Controller (support up to 4 SMD Disks with a total of 8 billion bytes)
- Parallel/Serial I/O
- Memory (up to 3 megabytes)

Options include:

- Data Base Accelerator (improves performance by a factor of 10)
- Expanded I/O capability: 64 serial or 8 GPIB lines
- Additional disk controllers: 4 total (maximum of 16 disks)

4.4.2 IDM-500 DBMS Description

The IDM-500 provides the user with a Relational DBMS capability. (Refer to section 4.4 for an explanation of a relational DBMS.) The IDM can manage up to 50 different data bases (each of which can contain up to 32K relations); relation size is limited to 250 different attributes (fields); tuples are limited to 2K bytes in length. As are the primary characteristics of relational DBMS, the IDM-500 provides the user and applications programmer with data structure/storage independence.

4.4.2.1 Overall Capabilities

In order to easily interact with the IDM-500, the following basic database commands are provided:

- Create (Destroy) a Database
- Create (Destroy) a Relation
- Retrieve Data
- Change Data
- Add (Delete) a Tuple
- Create (Destroy) an Index

Other DBMS management functions/utilities include:

- Logging
- Load and Dump Utility
- Database Protection
- Database "views"
- Multiple thread data base and system control
- Stored query for process optimization

IDM data types are: Binary Coded Decimal (BCD); 1,2, or 4 byte Integer; 4 or 8 byte Floating Point; Character (up to 255 characters); and Binary strings. Arithmetic functions include: addition, subtraction, multiplication, division, modulo, and absolute value. (Arithmetic functions can be applied to any BCD or Integer words). Aggregation verbs include count, count-unique, average, average-unique, maximum, minimum, sum, sum-unique, and any. The current time and date are also available to the user via a special function.

4.4.2.2 DBMS Command Capability

- Create Database - this command sets up the physical data base characteristics
- Open Database - allows access by users to a database
- Create Relation - creates the format for the relation/table defines data type and size
- Retrieve Into - allows data to be put into the database relation
- Range - defines limits for a data search

- Retrieve - display data
- Create Index - data is sorted on a "key" and that "key" is stored
- Create View - allows access to only a portion of the database
- Change Data Commands

  Replace - values in database are changed
  Delete - tuples are deleted
  Destroy - relation is removed

- Protection Commands

  Deny - locks out unauthorized users from the relation
  Permit - gives user access to a relation

4.4.2.3 DBMS Utility Capability

- Dump disk device - allows saving of entire database efficiently
- Load disk - converse of dump disk
- Dump/load Database - allows selective saving and loading of logical databases
- Dump transaction Log - saves the transaction accounting data
- Rollforward - based on the transaction; database is restored to a certain point in time

4.4.2.4 DBMS File Capability

- Create/destroy File - creates/destroys a file
- Open/close File - access to file is granted/released
- Read/write File - allow direct read/write access

4.4.3 User Interface

The IDM-500 system is complete unto itself; however, the user must supply the interface between the host computer and the IDM hardware. This interface can be furthur broken down into two parts: a user command language and a hardware device driver. Currently, the IDM-500 is only supported on the PDP-11/70 using UNIX.

The interface functions to be developed include:

- Provide user/terminal interface language
- Translate user oriented commands into IDM compatible format
- Transmit user commands to the IDM (device driver function)
- Receive IDM processed data and pass to user
- Format data for display to user

4.5 Voice Recognition and Response

Spoken language and sounds have not played a significant Man Machine Interface (MMI) role in Tactical Intelligence (or major C^3I) systems. Use has been limited to buzzers and electronic tones (normally monotone). Traditionally, synthesized human speech or voice recognition could only be accomplished by special purpose processors at great costs. Due to the decreased costs and increased power of microprocessors, voice capability is available to the system designer at minimum cost. The system previewed below is one of several commercially available systems that can be used to refine/redefine intelligence concepts in a laboratory environment.

4.5.1 Mike - Voice Recognition and Response

Mike is a commercial product of Centigram Corporation to provide audio I/O to digital systems. Mike provides a voice recognition capability by training the system to specified user voice inputs; the external response based on the voice input could be voice or signal to the computer to do a preprogrammed task. The basic system supports up to 16 isolated words or short connected phrases; expansion to the optional memory and disk system makes Mike's recognition power unlimited. A sensitivity threshold setting is offered for various degrees of assured success.

Mike also can digitize speech, store it, and "speak" back on command. Basic unit can store up to 8 seconds of speech; expansion can be accommodated by the use of the expanded memory and disk options.

4.5.2 Lisa - Voice Response

Lisa, also developed by Centigram Corporation, is the voice response module in the Mike device. This package allows the user to integrate voice into a system by plugging Lisa into the computer RS-232 interface and the user terminal (also RS-232) into Lisa. Special control characters are then embedded into user programs and "trapped" by the Lisa unit; sounds and voice are then produced using the "standard" vocabulary set provided by the company. Non-control characters are passed to the terminal in a normal manner.

4.5.3 VoiceWare - Voice Development System for MMI Applications

VoiceWare is a standalone unit used to create speech files for unique applications. Voice files created with this unit are used with Lisa. The system consists of a voice synthesizer, digitizer, microphone, terminal work station, disk, and software to support voice output applications. This package allows unique words and phrases (e.g. BE, TDI Cat, FRAG, etc.) to be incorporated into the evolving system without great expense or time.

Appendix A - Memory Optimization in the PDP-11/70

OBJECTIVE

This paper documents the procedures and results of optimizing the core/MOS main memory configuration on a Digital Equipment Corporation (DEC) computer system. This test was accomplished by reconfiguring the memory architecture so that the starting address of main memory (0000) was MOS vice core. This allowed operating system and most user tasks to be loaded and executed in high-speed MOS memory. Three software tests were employed as benchmarks to determine the relative increase in system performance and the type of task (memory diagnostic, I/O bound task, or CPU bound task) that benefited most from the change.

BACKGROUND

This experiment was conducted at the Tactical Operations Analysis Support Facility (TOAS Facility) at Langley Air Force, Virginia. The TOAS Facility is a TRW operated R&D computer system sponsored by the Rome Air Development Center (RADC).

PDP-11/70s purchased directly from DEC are configured with a minimum of 128K bytes (64K words) of main memory; this memory can be MJ11-A/B core or MK11 MOS. Due to lower cost, additional "add-on" memory is normally purchased from a non-DEC source and installed on the PDP 11/70. When this "add-on" memory is installed, it is usually "daisy chained" to the existing DEC memory. This practice keeps the lowest system addresses in the DEC memory. Therefore, the slower core memory is always used by the operating system before the faster MOS memory.

The TOAS System B PDP-11/70 memory configuration (see Figure 1) used in this experiment was first configured with the minimum amount (128K bytes) of DEC core and later expanded with "add-on" Intel 1670 MOS memory (896K bytes). Before memory reconfiguration the the MJ11 core memory occupied lower physical addresses (0000 - 400,000) and the IN-1670 MOS contained the higher (400,000 - 4,000,000) physical addresses.

System performance differences were expected due to the MJ11 core memory refresh cycle and the number/type of task using the core memory. Memory performance characteristics are given in Table 1 below.

Table 1. Memory access and cycle time comparisons.

Memory Type	Access Times	Cycle Times
MJ11-A	750 nS	1080 nS
IN-1670	555 nS	750 nS

The above figures support the premise that computer efficiency would be increased if the operating system tasks were loaded in the faster area of main memory.

The characteristics of the IAS V-3.0 operating system provided the incentive to perform this test. Investigation of the IAS operating system software reveals that certain system tasks are fixed in main memory after system start-up, and several important system tasks reside in the lower 128K bytes of the slower MJ11 core memory. A diagram of the operating system tasks occupying the lower 128K bytes of main memory is shown in Figure 2. These system tasks are always fixed at predetermined physical memory addresses regardless of the memory type.

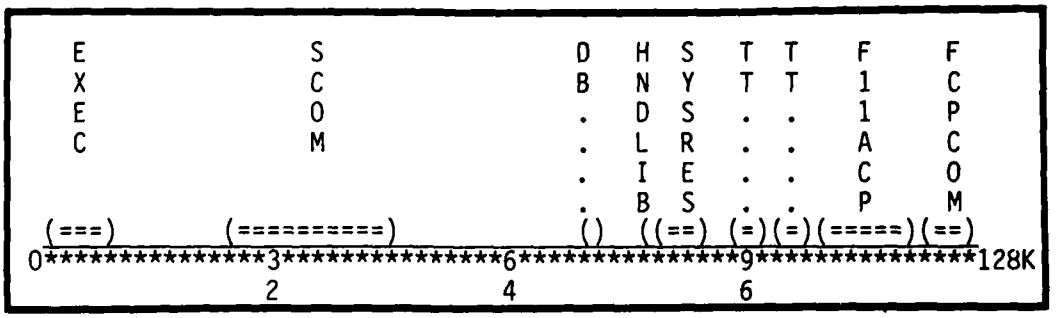


Figure 2. Diagram of the first 128K bytes of main memory with IAS V3.0 operating system resident.

METHODOLOGY

Experimental main memory configuration consisted of swapping the MJ11 core memory with the IN-1670 MOS memory. Standard and experimental memory configurations are shown in Figure 3.

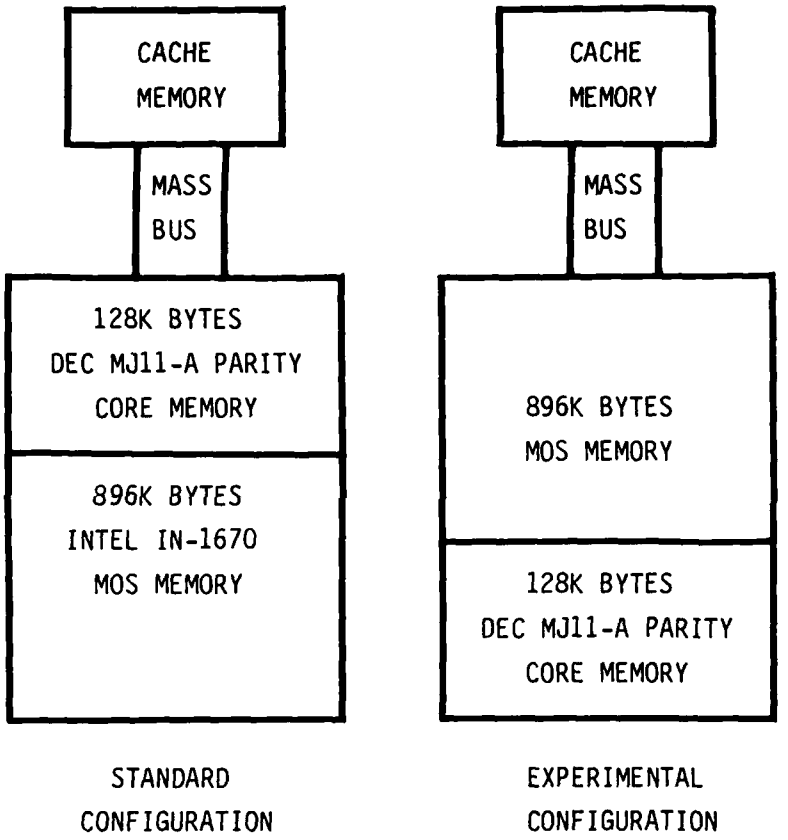


Figure 3. Standard and experimental main memory configurations.

Memory interleaving is another technique to increase system performance; however, this was not possible due to the incompatibility of the DEC and Intel memory boxs. After reconfiguration, the IN-1670 MOS occupied lower physical addresses (0000 - 3,400,000); the upper physical addresses (3,400,000 - 4,000,000) were MJ11 core memory. The actual memory reconfiguration required four hours to complete.

EXPERIMENTAL TESTING

Testing was accomplished by running three benchmark software tasks before and after memory reconfiguration. Increases in system performance were measured by decreases in task execution times. The timesharing system (IAS) was quiescent except for one user terminal logged in for the purpose of executing two of the three tasks. The IAS operating system was not needed to execute the diagnostic task. The benchmark tests are described as follows:

- Memory Diagnostic - DEC memory diagnostic, EMKA, is designed to test and verify all main memory functions as quickly as possible. The program is loaded into lower core and checks all main memory above this point. After completing upper memory, the program relocates out of lower core memory and completes testing the lower core previously occupied. This diagnostic was used primarily to verify successful memory operation after reconfiguration.
- Arithmetic Calculations - This small task calculated all prime numbers from zero to 5,000. The program did not require disk transfers and was "compute bound".
- Data Base Operations - The relational data base management system, Oracle, was installed in the timesharing system and a series of data base queries were executed via command file. This task requires many disk transfers and was therefore, heavily "I/O bound".

RESULTS

Test results indicated that all benchmarks exhibited some degree of decreased execution time and increased system throughput. Table 2 contains the results of the benchmark task executions.

Table 1. Benchmark task execution times before and after main memory reconfiguration.

Task Name	Task Size	CPU Time in Seconds Before/After	Execution Time in Seconds Before/After	Percentage Increase
EMKA	-	- / -	687.0 / 677.0	3.0 %
Prime	9K	158.8 / 156.8	- / -	1.2 %
Oracle	29K	6.9 / 6.7	150.0 / 139.0	7.3 %

The memory diagnostic, EMKA, executed faster in the experimental configuration. Execution speed was increased because EMKA runs primarily in the lower end of memory which was faster MOS memory after reconfiguration.

Oracle data base queries exhibited the largest percentage of execution speed increase. The most probable reasons for this is linked to the over-all operating system speed. With the Oracle tasks installed in the operating system, the scheduler (integrated into the executive) was able to increase task scheduling because the executive now resided in faster IN-1670 MOS memory. I/O wait time was also reduced because three main I/O tasks were now also resident in IN-1670 MOS memory.

The compute bound prime number generator task exhibited execution time decrease but to a smaller degree. By being very short, (12 lines of FORTRAN code), this program allowed the high speed cache memory to maintain a high hit rate and did not require many main memory cycles. The increased execution speed is mostly attributed to the executive operating in MOS memory.

CONCLUSIONS

System throughput was increased by reconfiguring the core/MOS main memory configuration in a manner that allowed the total IAS operating system to reside in the faster IN-1670 MOS instead of occupying the slower MJ11 core memory. The system areas exhibiting the largest efficiency increase were those involving the I/O tasks (DB...., F11ACP, and FCPCOM). Since the Oracle benchmark is more typical of a loaded operating system where large amounts of disk I/O are taking place, memory reconfiguration could be important and beneficial in other computer systems of similar memory configuration and task requirements.

LIST OF REFERENCES

The following documents were used as references in the production of this report:

Digital Equipment Corporation (DEC) Publications

1. PDP-11/70 Maintenance and Installation Manual
   EK-11070-MM-001, 1977
2. PDP-11/70 System User's Manual
   EK-11070-OP-001, 1971
3. PDP-11 Software Handbook
   EB-18687-20, 1978
4. KB11-C Processor Manual (PDP-11/70)
   EK-KB11C-TM-001, 1971
5. PDP 11 Processor Handbook
   EB17716-18/79, 1979
6. FP 11-C Floating Point Processor Maintenance Manual
   EK-FP11C-MM-001, 1976
7. FP 11-C Floating Point Processor User's Manual
   EK-FP11C-OP-001, 1976
8. PDP 11 Peripherals Handbook
   EB-05961-76, 1976
9. Peripherals Handbook
   EB-18293-20/80, 1980
10. M9312 Diagnostic ROM documentation
11. MJ 11 Memory System Maintenance Manual
    EK-MJ11-MM-002, 1976
12. MJ 11 Memory System User's Manual
    EK-MJ11-OP-001, 1976
13. RWP05/RWP06 Moving Head Disk Subsystem Maintenance Manual
    ER-RWP56-MM-00, 1976
14. RWP05/RWP06 Moving Head Disk Subsystem User's Manual
    EK-RWP56-OP-001, 1976
15. RWP05/RWP06 Device Control Logic Maintenance Manual
    EK-RP056-MM-001, 1975
16. RP05/RP06 Device Control Logic User's Manual
    EK-RP056-OP-001, 1976

17. RP05/06 DEC Disc Storage Drives Technical Manual (Memorex Corp)
677-01151.20-01, 1976

18. TE16/TE10W/TE10N DEC Magtape Transport Maintenance Manual
EK-OTE16-TM-001, 1976

19. TE16/TE10W/TE10N DEC Magtape Transport User's Mannual
EK-TEWN-OP-001, 1976

20. TMB11/TU10W DEC Magtape System Maintenance Manual
EK-TMBEF-MM-001, 1976

21. TMB11/TS03 DEC Magtape System User's Manual
EK-TMB11-OP-001, 1976

22. Model 2230 Line Printer (Data Products Corporation)
DPC-241735F, 1978

23. LP11/LS11/LA11 Line Printer Manual
EK-LP11-TM-006, 1976

24. LP11/LS11/LA11 Line Printer User's Manual
EK-LP11S-OP-001, 1976

25. CR11/CM11 Card Reader System Manual
EK-CR11-TM-004, 1976

26. CR11/CM11 Card Reader User's Manual
EK-CR11-OP-001, 1976

27. PC11 High Speed Reader Punch and Control Manual
EK-PC11-TM-003, 1974

28. Roytron 500 Series Reader/Punch Mechanisms
Roytron-ER-00015, 1966

29. PC11 High Speed Reader Punch and Control User's Manual
EK-PC11-OP-001, 1976

30. Terminals and Communications Handbook
EB-15486-20/79, 1979

31. LA34 User's Guide
EK-OLA34-UG-CN1, 1978

32. LA35/36 DECwriter II Maintenance Manual Volume II
EK-2LA36-MM-001, 1976

33. LA36/LA35 DECwriter II User's Manual
EK-LA36-OP-001, 1977

34. VT100 Series Technical Manual
EK-VT100-TM-002, 1980

35. VT100 Tempest User's Manual
EK-VTTMP-UG-001, 1979

36. DF02 Modem User's Guide
EK-ODF02-UG-002, 1980

37. DL11 Asynchronous Line Interface Manual
EK-DL11-TM-003, 1975

38. DL11 Asynchronous Line Interface User's Manual
EK-DL11-OP-001, 1976

39. Diagnostic CZQXALO XXDP User's Manual
AC-9093L-MC, 1978

40. IAS System Management Guide
AA-2502D-TC, 1978

41. Diagnostic CXQUAAO DEC X 11 User's Manual
AC-F053A-MC, 1978

42. DZ11 Maintenance Manual
EK-DZ11-MM-PRE, 1977

43. DZ11-X Asynchronous Multiplexer Technical Manual
EK-DZ11-TM-001, 1979

44. IAS/RSX Diagnostic Reference Manual
DEC-11-OXLDA-C-D, 1977

Beehive International

45. B500 Computer Terminal Operator Manual
TM96-8501C, 1974

Bell Telephone Laboratories Inc.

46. Documents for the PWB/UNIX Time-sharing System
Edition 1.0, 1977

47. Unix Time-sharing System: The Programmer's Workbench
The Bell System Technical Journal, 1978

Britton-Lee Inc.

48. IDM 500 Intelligent Database Machine
Product Description, 1981

49. IDM 500 Software Reference Manual
Version 1.3, 1981

Bunker Ramo Corporation

50. BR-1566 Memory Bus Interface Unit
TM-MIU-1566-01, 1980

51. BR-1569 Communication Control Unit Volume I
TM-CCU-1569-02-1, 1978

52. BR-1569 Communications Control Unit Volume II
TM-CCU-1569-02-2, 1978

Chromatics

53. Chromatics CGC-7900 Color Graphics Computer System User's Manual 070201, 1981

Conrac Monitors

54. Conrac Installation, Operation, and Maintenance Manual IB-106122-999, 1976

Data Systems Design Inc.

55. DSD 210 Diskette Memory System General Product Description, 1976

Genisco Computers

56. System Description Manual CGT-3000 Series Display Systems 3000SD-01, 1976

57. Programmable Graphic Processor Manual 3011-01, 1976

58. CGT-3000 Interface Reference Manual 3000IR-01, 1976

59. Memory I Maintenance Manual 3021-00, 1976

60. Video Control Maintenance Manual 3031-01, 1976

Imlac Corporation

61. PDS-4 Display Maintenance Manual IM-474771-0100, 1978

62. Model D3300 and D3400 Disk Drives (Pertec) PER-104615, 1978

63. Imlac Diagnostic Packages

ROMLOD	472611-3110
RDISK	542211-3503
TTAPE1	572231-1601
TTAPE2	572211-1602
TTAPE3	572211-1603
TTAPE4	472231-1604
TTAPE5	572231-1605
TTAPE11	472231-1611

64. Programming Guide to Imlac IM-544121-3502, 1976

Precision Visuals Inc.

65. DI-3000 User's Guide, 1981

Relational Software Inc.

66. Oracle Introduction - Version 1.5
RSI-110, 1979

67. Oracle Programmer's Guide - Version 2.3
RSI-100

Sperry Univac Corporation

68. Univac 1652M Technical Manual
PX-12494 Vol I, 1978

69. Dual Monitor Terminal Operator's Manual
PX-12323, 1978

70. Dual Monitor Terminal Microprocessor Programming Manual
PX-12588, 1978

71. Dual Monitor Terminal Host Computer Programming Manual
PX-12324, 1978

System Industries

72. System Industries Technical Manual Volume One
9400-11-01, 1980

73. Model 9400 Disk Storage System Software Manual
PB9400-9001-04

74. 94DIAG User's Manual, 1980

Other Doucumentation

75. 32-Bit Minicomputer Achieves Full 16-Bit Compatibility
Computer Design, 1981

76. DEC DL11-E/Univac 1652 Interface Software Specification
OSI-N80-003, 1980

77. More Light on Optical Fiber Systems
Demodulator (GTE), 1981

78. Latest in Disk Technology
Electronic Design, 1980

79. Fiber Optic Components Improve At Both Ends
Electronic Design, 1981

80. Microprocessor Tables: General-purpose, All-in-one, Bit-slice,
Alternative Sources
Electronic Design, 1981

81. Bubble Memory Basics
Fujitsu, 1979

82. Opto-electronics Designer's Catalog
Hewlett Packard, 1981

83. Disk-Storage Technology
Scientific American, 1981

84. Program Load Module Documentation
Sperry Univac, 1980

85. Experiences with the UNIX Time-sharing System
J. Lions, Department of Computer Science,
University of New South Wales, Kersington, Australia, 1978

AD-A116 841 TRW DEFENSE AND SPACE SYSTEMS GROUP MCLEAN VA F/G 15/7
TACTICAL OPERATIONS ANALYSIS SUPPORT FACILITY,(U)
MAY 82 M P MURPHEY, D E YUCHNOVICZ, R W STARR F30602-78-C-0196
UNCLASSIFIED RADC-TR-82-15 NL

2 OF 2
AD A 116841

END
DATE FILMED
8-82
DTIC

GLOSSARY

Access	Seeking, reading, or writing data on a storage device
Access method	Techniques for locating data (e.g. serial access, random access, remote access, virtual sequential access method (VSAM), hierarchial indexed sequential access method (HISAM)
Access time	The time that elapses between an instruction being given to access data and that data being available for use
Address	An identification (number, name, label) for a location in which data is stored
ADP	Automated Data Processing
Algorithm	A computational procedure or technique
AM	Amplitude modulation
Amplitude Modulation	Method of signal transmission in which the amplitude of the sine wave carrier signal is changed in accordance with the information to be transmitted
Analog signal	A signal that has the form of a continuously varying physical quantity, i.e., voltage
ASCII	American Standard Code for Information Interchange - an eight level code
ASR	Automatic Send-Receive teletypewriter machine
Assemble	To convert a routine coded in a higher level computer language into actual machine language instructions
Associative storage	Storage which is addressed by content rather than by location
Asychronous transmission	Start-stop transmission; transmission in which each information character (word or block) is individually synchronized by use of a start and stop elements
Attribute	A field containing information about an entity
Baud	Unit of signaling speed; normally the same as bits per second

Baudot	Five bit, 32 character code used by some TTY transmission systems
BCD	Binary Coded Decimal - a six bit alphanumeric code
Binary code	An electrical representation of information expressed in the base two number system
Binary search	A method for searching a sequential file/table; procedure is based on algorithim that divides data into two equal groups and determines which group contains the required data and then repeats procedure with that group
Bit	A contraction of the words "binary digit" - smallest amount of information that can be represented (normally thought of as a one or zero)
Blocking	Combining two or more records so that they are jointly read or written by one machine instruction
BPS	Bits per second
bpi	Bits per inch
BR-1566	Massbus controller used to interface the BR-1569 to the PDP-11/70
BR-1569	Communications multiplexer that supports 8-32 channels-manufactured by Bunker Ramo - part of baseline configuration
Byte	A group of data handled as a unit (commonly 8 bits is to one byte)
Cache memory	High speed memory placed between slower main memory and the processor; cache increases effective memory transfer rate
CATIS	Computer Aided Tactical Information System
chaff	Small, light scraps of paper tape
chip	The substrate on which LSI circuits are fabricated; sometimes referred to as the circuits themselves
Circular buffer	A queue that has front and rear pointers to keep track of information in a defined area
Circular file	An organization for a file of high volatility, in which new records being added replace the oldest records

CODASYL	Conference of Data Description Languages; DBMS type
Concatenate	To link together - a concatenated data set is a collection of logically connected data sets
Control character	A character whose occurrence initiates, modifies, or stops an on-going operation
CPU	Control Processing Unit
Cylinder	A concept of storage using magnetic disks - a area read without moving the arms of the disk drive
DASD	Direct Access Storage Device
Data	Numbers, text, fact, information which are represented in a formal structure so that it can be processed by computers
Data administrator	An individual with an overview of an organizations data base
Data base	A collection of interrelated data stored together to serve one or more applications
Data base management system	The collection of software required for using the data base
Data dictionary	A catalogue of all data types giving their names and structures
Data structure	Well defined format and access conventions associated with a particular class of information
Db, db	Decibel
DBCS	Data Base Control System
DBMS	Data Base Management System
DCL	DEC Command Language
DCL	Device Control Logic
DEC	Digital Equipment Corporation
Decibel	A unit for measuring relative strength of a signal parameter such as power, voltage etc
DEC/X-11	A configurable system exerciser diagnostic program in the MAINDEC-11 diagnostic package

DDL	Data Definition Language
Demodulation	The process of retrieving data from a modulated carrier signal - the opposite of modulation
Diagnostic	A program that tests logic and reports any faults it detects
Direct access	Retrieval or storage of data by a reference to its location on a volume, rather than relative to the previously retrieved or stored data
DL 11E	Single line asychronous interface manufactured by DEC
DMA	Direct Memory Access
DPU	Display Processing Unit
DVM	Digital Volt Meter
EBCDIC	Extended Binal Coded Decimal Interchange Code; an eight bit alpha-numeric code
ECC	Error Correction Code
EDP	Electronic Data Processing
EIA	Electronics Industry Association
EIA Interface	A standard set of signal characteristics (time duration, voltage, and current) specified by the Electronic Industries Association
Error-correcting Code	A code having a sufficient number of signal elements to allow error detecting and/or correcting at the receiving station
Even parity	A check (or count) of a block of data to insure that an even number of bits are contained in the block
Fatal Error	An error in a system or program that inhibits any further system operation or program execution
FDM	Frequency Division Multiplex
FDX	Full Duplex
Fiber Optic Waveguides	Filaments of glass through which a light is transmitted for long distances by means of internal reflections
Field	A set of contiguous bytes in a record

FM	Frequency Modulation
FPP	Floating Point Processor
Frequency	The rate at which a current alternates
Frequency division multiplex	multiplex system in which the available transmission frequency range is divided into narrower bands
Frequency modulation	Method of modifying the frequency of the sine wave carrier to support information transmission
Full Duplex	Equipment capable of transmission simultaneously in two directions
Gate	A basic logic circuit
Half Duplex	A circuit that can transmit information in both directions, but not simultaneously
Hamming Code	A error correcting/detecting code using redundant bits
Hertz	A unit of frequency measurement, i.e., one hertz equals one cycle per second
HD	Half Duplex
Hollerith code	A alphanumeric code used in card readers and sorters
Hz	Hertz
IAS	Interactive Applications System
IC	Integrated Circuit
Index	A table used to determine the location of a record
Intelligent terminal	A terminal that can perform data processing/manipulation tasks without relying on the host computer
Interface	The boundary between two pieces of equipment: consists of physical characteristics, signal strengths, information codes, protocols etc
Interleaved	Assigning consecutive physical memory addresses alternately between two memory controllers
Inverted file	A file structure which permits fast spontaneous searching for previous unspecified information - independent lists or indices are maintained in records keys which are accessable according to the values of specific fields

I/O	Input/Output - refers to computer generated information displays and input
I/O channel	An equipment that forms part of the input/output system
ips	Inches per second
KSR	Keyboard Send Receive teletype machine
LA-36	30 characters per second dot maxtrix printer commonly used as a console device
Label	A set of symbols used to identify an item, record, message or file
LED	Light Emitting Diode
Link	The process of connecting object modules into a contiguous executable task
List	An ordered set of data items, a chain
Logical	Data organization, hardware, or system that is perceived by the applications programmer, different from real (physical) form
Longitudinal redundancy check	A method of checking the reliability of a block of data
LRC	Longitudinal Redundancy Check
LSI	Large Scale Integration; method of placing many electronic circuits on one small chip
MAINDEC-11	A system diagnostic package containing the XXDP monitor and system component diagnostics.
MASSBUS	36 bit wide data path between the CPU, memory and high speed peripherals
MDLI	Minimum Device Level Interface
Mbyte, MB	Mega-byte; 1,000,000 bytes
Mean time to failure	The average length of time for which the system or component works without failing
Mean time to repair	Average time required to repair the system or component

MHz	Megahertz - a unit of frequency measurement equal to one million hertz
mil	Measurement of thickness; 0.001 inch
MODEM	Modulator-Demodulator; a device that can modulate a signal for transmission and demodulate for reception
Modulation	A process of changing the characteristics of the carrier signal to reflect the values of the transmitted data
MOS	Metal Oxide Semiconductor; a type of LSI chip
MPG	Maintenance Program Generator
MSI	Medium Scale Integration; solid state technology with fewer circuits per chip than LSI
MTTF	Mean time to failure
MTTR	Mean time to repair
Multi-access	The capability to allow several users simultaneous access to the computer
Multiplex	Using a common channel to support more than one process or user by dividing the frequency band into narrower bands (FDM) or using time slots (TDM)
Multiplexer	A device that enables more than one signal to be sent simultaneously over one physical circuit
Multiprogramming	The method which supports several independent jobs processed together to maximize system performance
Multi-thread	The ability of a process (normally a data base management system) to support more than one user accessing a file or portion of code
MUSDAB	Multi-Source Data Base - Avanced R&D data base/effort to support Project 2315
Node	A point of junction between links - a switching or processing center
On-line	A device that is connected directly to the computer; normally thought of as an interactive device
Parity check	The process of adding non-information bits to a block of data to make the total number of bits even or odd

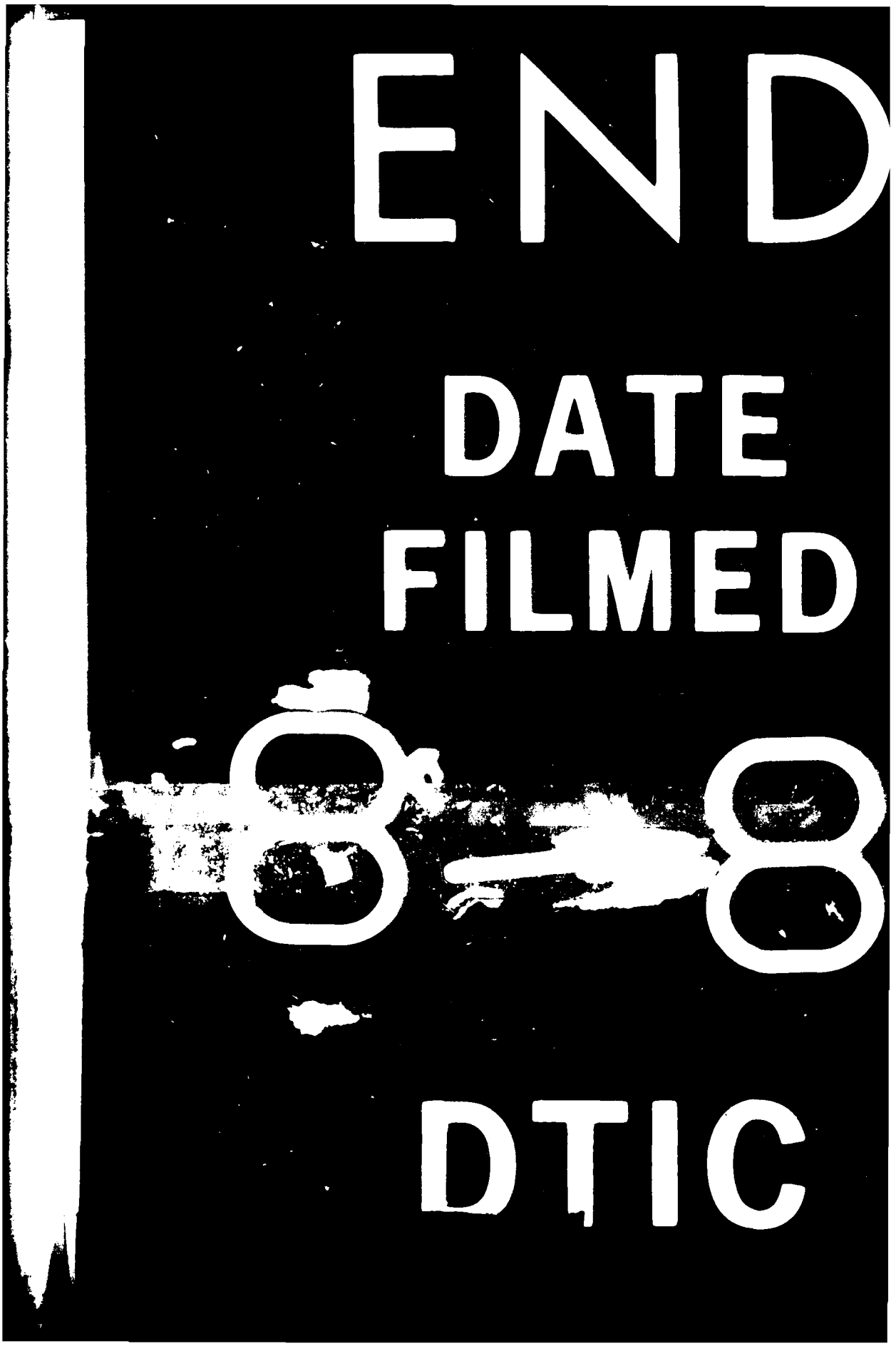
PDP 11/70	Programmable Digital Processor; the 11/70 is the most powerful 16 bit minicomputer in the DEC 11 series family of processors; part of TOAS baseline configuration
PDS-4/L	Stand-alone graphic refresh CRT terminal - part of baseline configuration; manufactured by Imlac
Peripheral device	Input or output devices of a computer (i.e. printers, magnetic tape drives, disks, consoles, CRTs, etc)
Peripheral interface	A standard interface between the computer and its peripherals designed to accommodate changes
PMI	Preventive Maintenance Inspection
Protocol	A fixed procedure required to initiate and maintain a communications process
RADC	Rome Air Development Center, Griffiss AFB, NY
RAM	Random Access Memory
Random access	The ability to access data directly without searching through other extraneous data
Real time	A process or transmission which occurs sufficiently fast that it is used in essentially the same manner as if it were instantaneous
Redundancy check	An automatic or programmed check based on characters used especially for checking purposes
Response time	The time the system takes to react to a given command or execute a particular process
RH-70	Massbuss controller for high speed peripherals
RF	Radio Frequency
RFI	Radio Frequency Interference
RO	Receive Only
ROM	Read Only Memory
RP06	A dual access moving head disk system; each pack can store 176 MB; part of TOAS baseline configuration
RS-232 Interface	An EIA standard for interfacing terminals and computer equipment

Seek	The mechanical movement of the flying head involved in locating a record on a random access device
Semaphore	A mechanism for synchronizing a set of processes; used to preclude one process from changing data (or code) being used by another process
Serial	An interface in which the bits of data are transmitted or processed one at a time
Simplex circuit	A circuit that allows transmission in a single direction only
Soft copy	A temporary record - normally associated with a CRT display unit
SPC	Small Peripheral Controller
Stop bit	The signal characteristic that denotes end of transmission
SU-1652	A dual screened CRT developed by Sperry Univac and used in the automated intelligence community
Synchronous	Having a constant time interval between successive bits, characters, or events
Task	A linked group of object modules ready for execution
TDM	Time Division Multiplex
TDMA	Time Division Multiplex Access
Teletype	Trademark of the Teletype Corporation that produces tape punches, page printers, etc used for communications systems
Throughput	The total amount of useful information processed during a specified interval
Time division multiple access	Physically separated devices are allowed access to a single device by allocating time slots to each one
TOAS	Tactical Operations Analysis Support Facility - the RADC test and demonstration facility at Langley AFB, Virginia
TTY	Teletype
UIC	User Identification Code
UFD	User File Description

UNIBUS	18 bit data path connecting all DEC peripheral devices to the 11/70 CPU
Virtual	Adjective implying that something in reality is different than it appears to a set of programs or users
Virtual storage	A technique that allows users to employ a computer as though it has a much larger memory than its real memory capacity
VRC	Vertical Redundancy Check
Word	A sequence of bits or characters treated as a unit; two bytes (16 bits) is one DEC 11/70 word
WPM	Words per minute
Xerox 1750	45 CPS letter quality daisy wheel printer - part of TOAS baseline configuration
XXDP	The "catch-all" name for the diagnostic programs contained in the MAINDEC-11 diagnostic package

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.


END
DATE
FILMED
8
8
DTIC